

ZPD Project Status¹

4 April 2003

For the *BABAR DCT Upgrade Final Design Review*

The Z- P_T Discriminator (ZPD) is a replacement of the P_T Discriminator (PTD) of the BABAR Level-1 Drift Chamber Trigger (DCT) system. In addition to the PTD's ability to select charged tracks based on their transverse momentum (p_T), the ZPD can use the tracks' origin (z_0) along the beam axis in order to reject the tracks that are not originating from the beam interaction point.

The initial design of the ZPD system was proposed at the Conceptual Design Review (CDR). The project has made significant progress since the CDR: prototype modules have been produced, the firmware code has been developed, and various tests have been performed to validate and improve the design.

This document provides a brief summary of the status of the ZPD project. Details of the current design and proposed implementation for the final ZPD modules can be found in the separate documents presented at this review.

1 Changes Since the CDR

Algorithm / Firmware

- No significant changes.

PCB

- Fix power via connections on PCB.
- Replace the FPGA configuration method.
- Route clock signals into the Decoder/Driver FPGA on dedicated clock pins.
- Minor changes for better labels, test points, etc.

2 Checklist Before Final Production

Verify PCB design is correct – done

- All on-board signals have been tested at full speed.
 - High speed and backplane I/O parts have received the most attention.
- Tests revealed problems to be fixed:
 - FPGA configuration method.
 - Clock input pins on FPGA.

¹ <http://www.slac.stanford.edu/BFROOT/www/Detector/Trigger/upgrade/fdr/zpd/ZpdStatus.pdf>

Verify that firmware will fit in the FPGAs – done

	Decoder/Driver Xilinx Virtex-II 3000	Finder/Fitter Xilinx Virtex-II 4000	Decision Module Xilinx Virtex-II 1000
Logic blocks	27%	44%	70%
RAM blocks	15%	74%	32%
Multipliers	not used	20%	not used

Verify that the firmware will run at full speed – almost done

- Complete design works stably at 60 MHz.
 - Xilinx software claims ~60.5 MHz.
 - It actually worked up to 67 MHz in a preliminary test.
 - Will follow up with more tests to ensure 10% margin.
- Limiting factor is the multipliers in Finder/Fitter.
 - Production version will have 2x faster multipliers.
- Next factor: routing delays of data bus between the Finder/Fitter memory blocks.
 - Not fundamental – can be fixed with loosening specific timing constraints.

Verify that there are no show stoppers in design

3 Issues Encountered So Far

- Almost all delays in firmware due to Xilinx or Leonardo software bugs.
 - Xilinx configuration solution (SystemACE MPM → CF helps).
 - Leonardo: incorrect implementation of subtractions in one version, multiplications in another.
 - Xilinx Place-and-Route code has been lacking in speed and intelligence.
 - Required much human intervention to make the timing constraints.
- Timing problem due to the placement of cclk and dclk inputs.
 - Will be fixed in the production version.