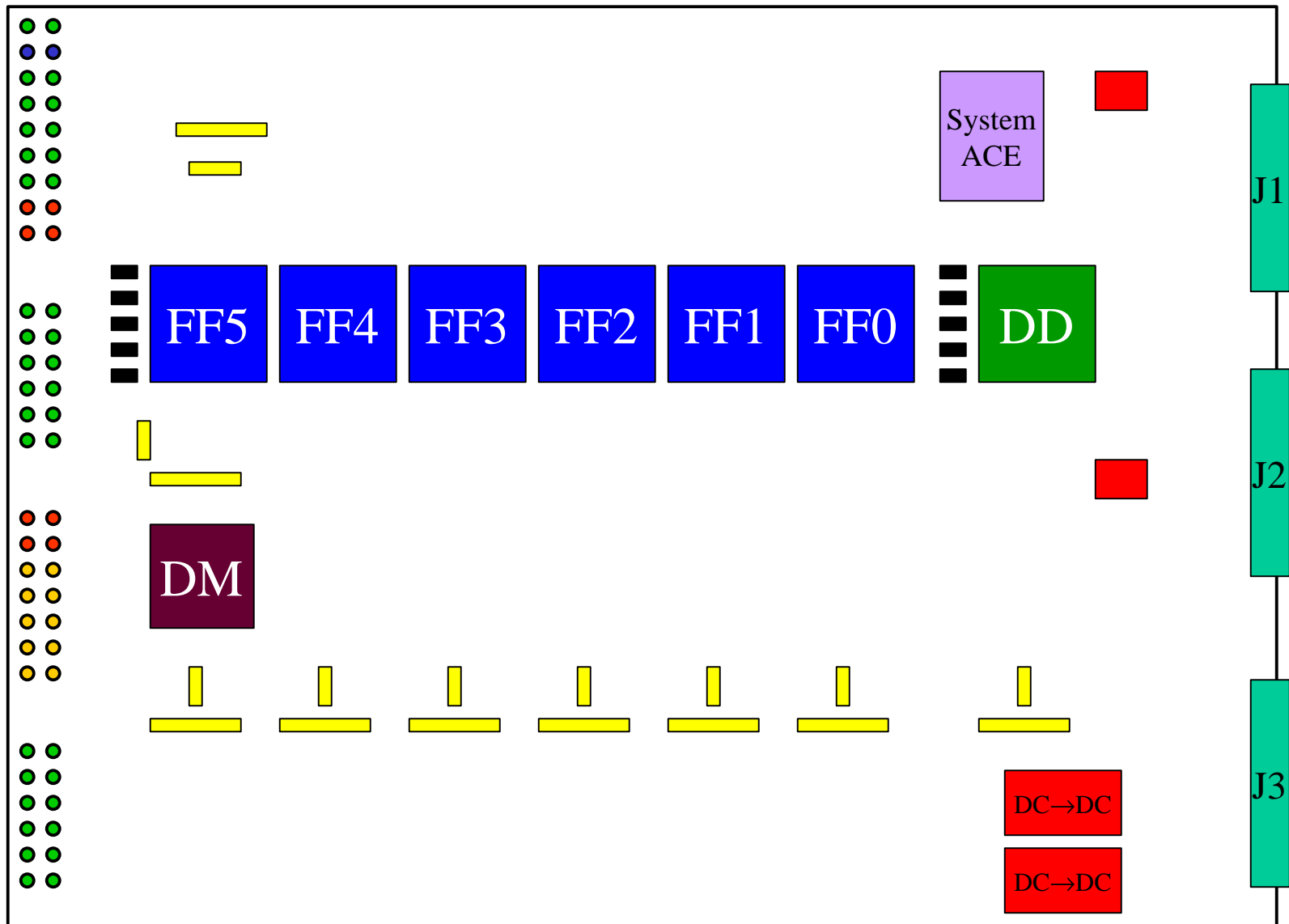
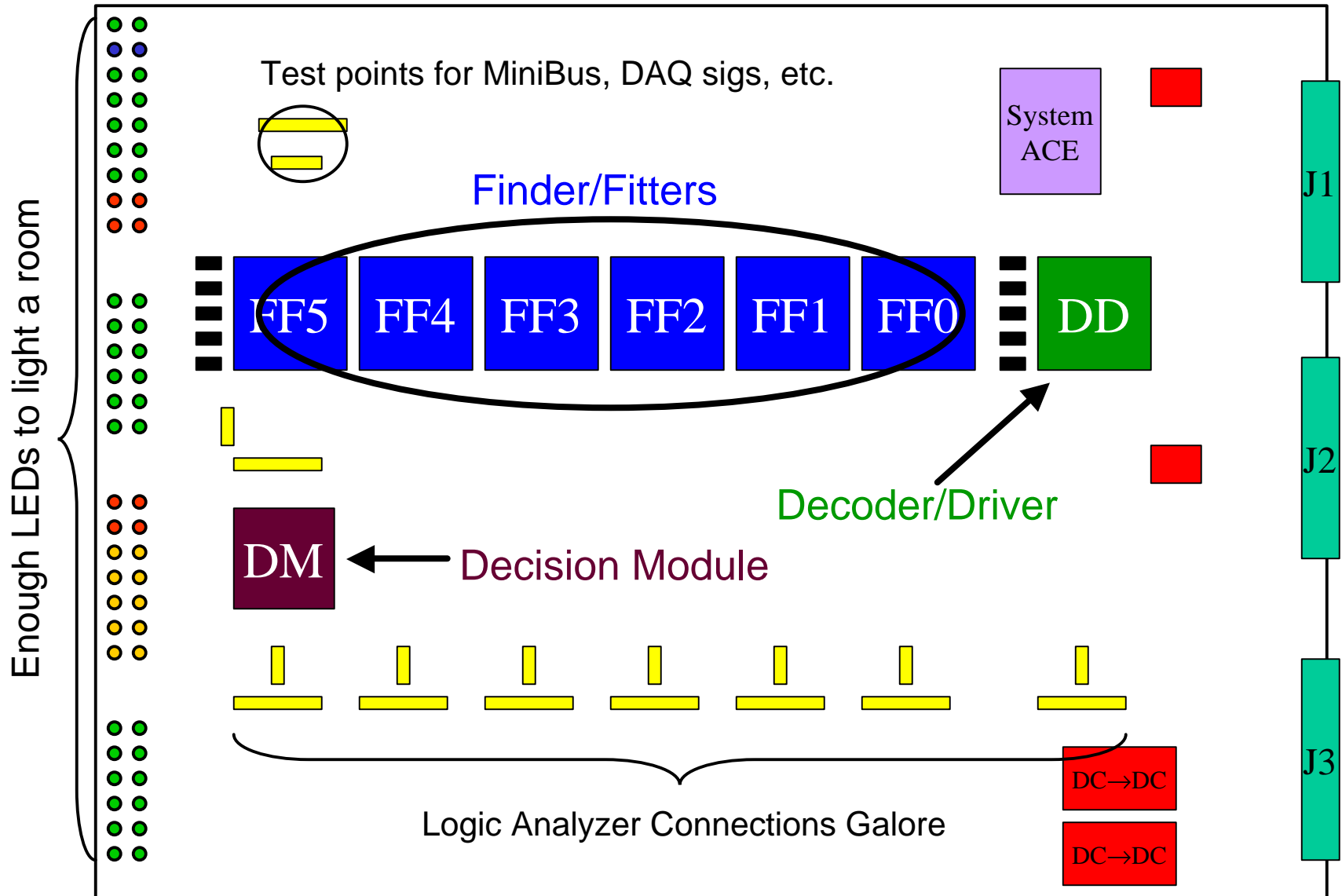


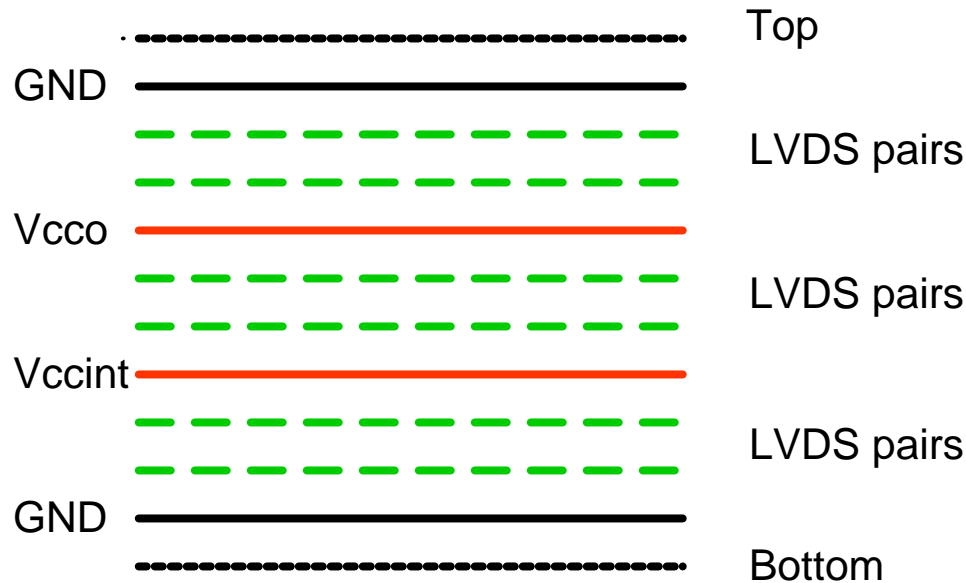
The Cartoon Guide to the ZPD



Layout

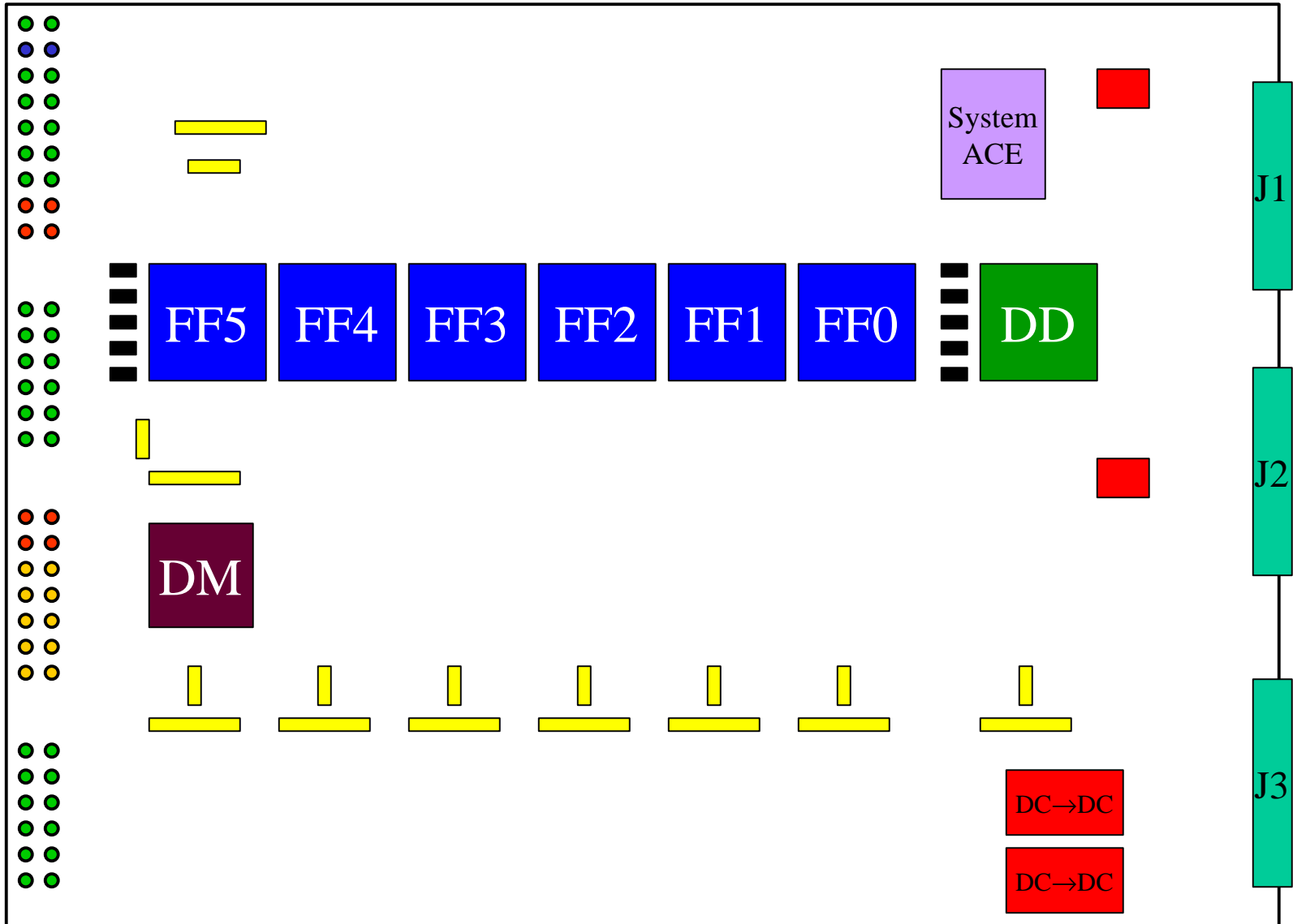


Layer Structure

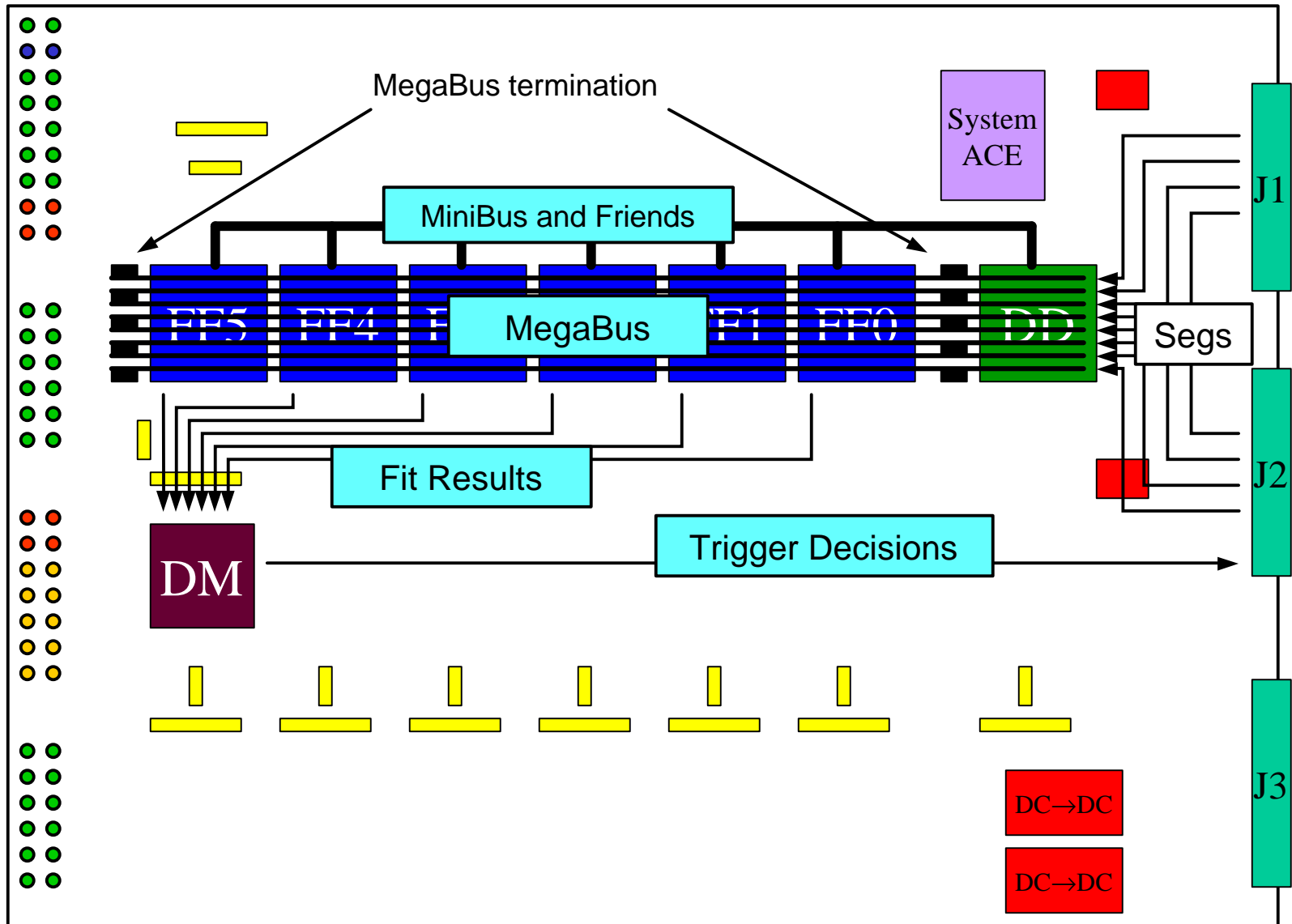


- Slow signals run on top and bottom
- High speed (120 MHz) Megabus runs on LVDS pairs
- Medium speed (30-60 MHz) signals and buses (MiniBus, FitResults, etc.) are on sides of LVDS pair layers

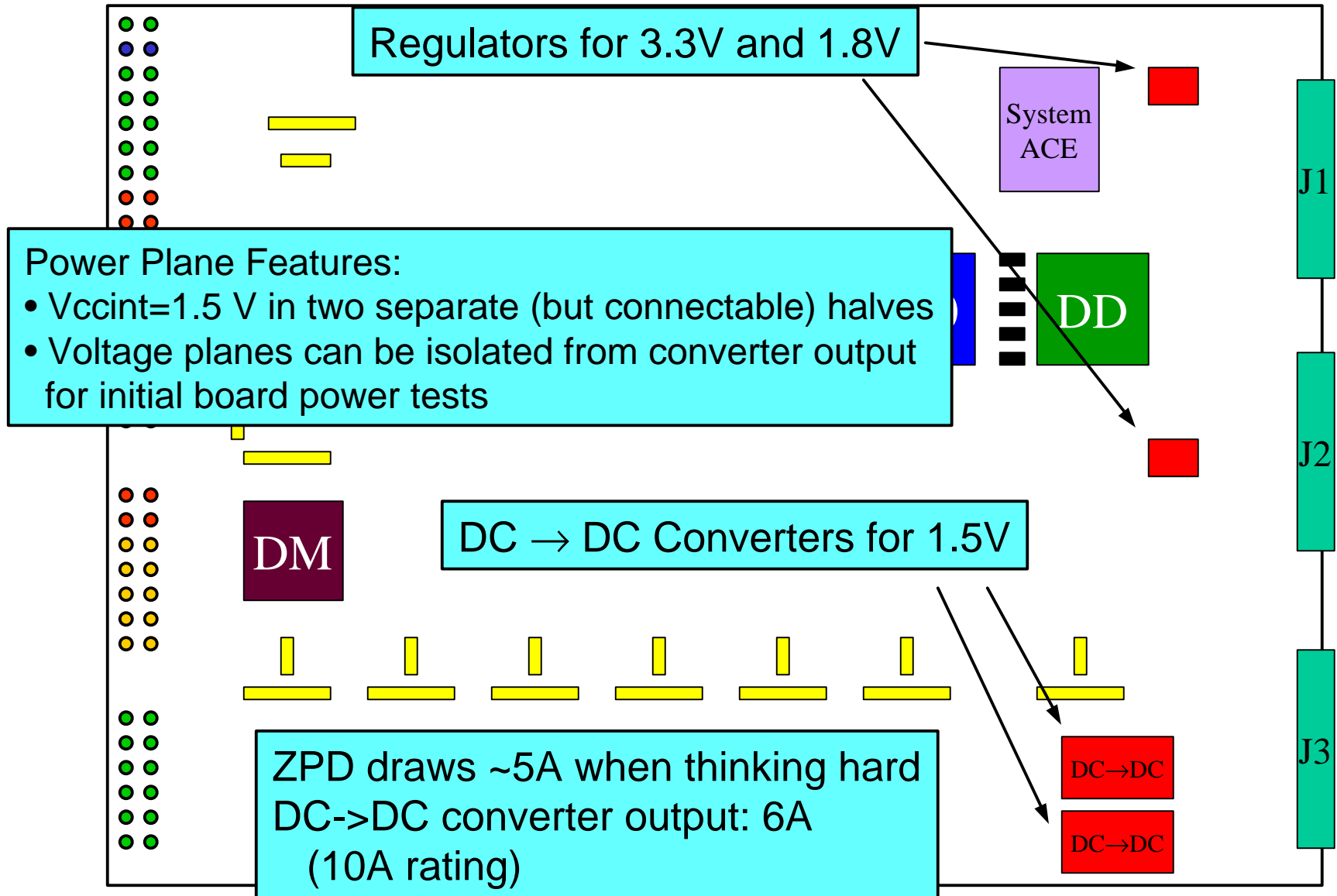
Layout (continued)



Signal Flow



Power



Regulators for 3.3V and 1.8V

System ACE

Power Plane Features:

- Vccint=1.5 V in two separate (but connectable) halves
- Voltage planes can be isolated from converter output for initial board power tests

DC → DC Converters for 1.5V

DM

ZPD draws ~5A when thinking hard
DC->DC converter output: 6A
(10A rating)

DC→DC

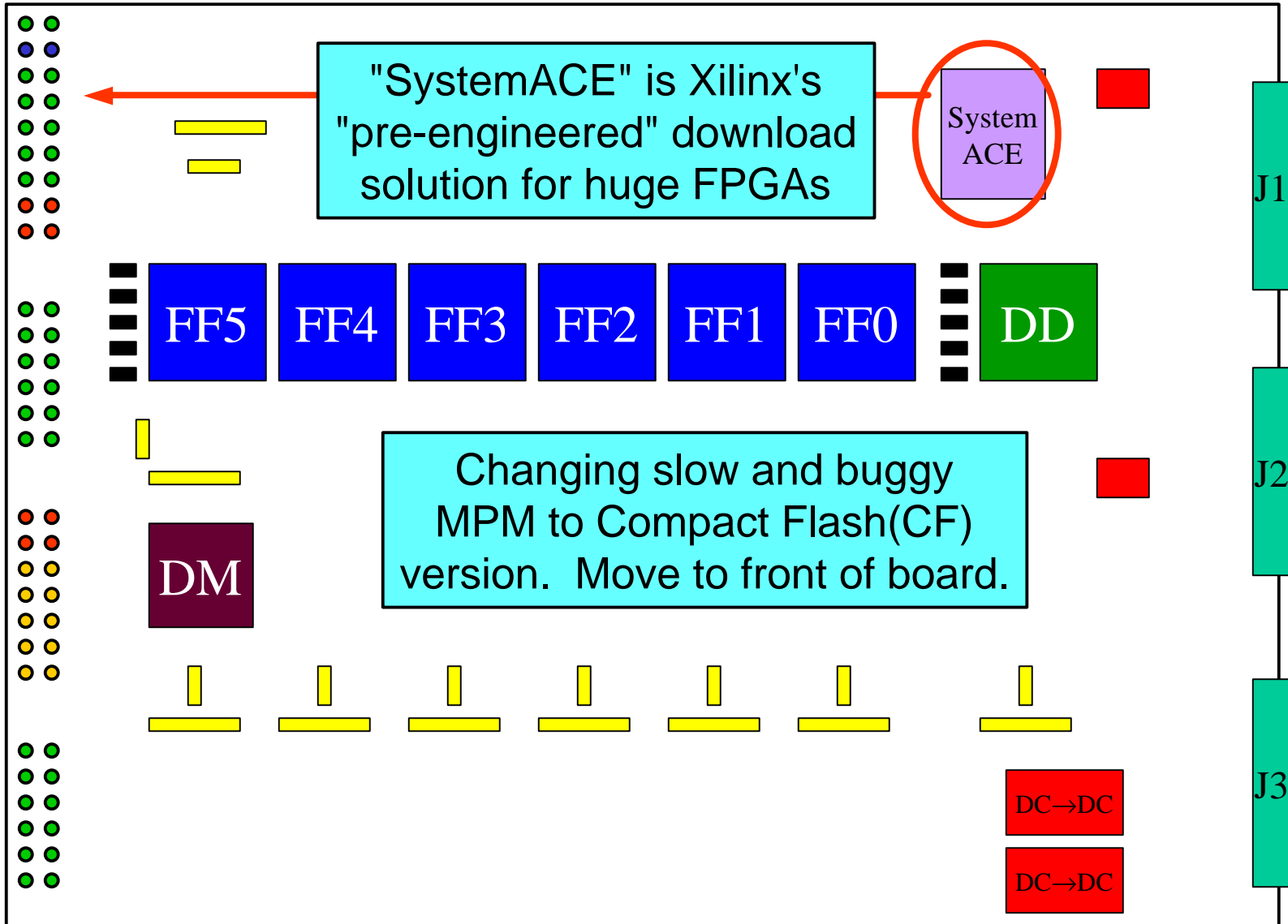
DC→DC

J1

J2

J3

FPGA Configuration



Changes from Prototype

- In general, the prototype PCB works well
- Need to fix power via problem which was due to bug in Gerber file generation software
- Other changes based on experience with prototype:
 - Better FPGA download method
 - Input Decoder/Driver clocks on dedicated clock pins
 - Minor improvements to labels, test points, etc.

Bottom line:

- We could use the prototype PCB as is
- Power via fix will improve long term stability
- Other changes will simplify our lives