ZPD Test Plan[1]

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This document describes the plan for testing the ZPD modules. The scope is limited to the board-level (as opposed to system-level) testing, i.e. what can be done without connecting the module to the rest of the DCT system such as the TSF modules and the GLT module.

1 Overview

The goal of the board-level testing is to uncover and fix potential problems that fall broadly into the following categories:

- Errors in the PCB design and layout,
- Failures in the PCB fabrications and assembly,
- Parts failures such as defective FPGAs, and
- Logic errors in the FPGA firmware.

Most of the problems listed above should be caught before the modules are produced. The PCBs are 100% tested against the net-list by the manufacturer. The assembly is preceded by a process optimization in which mechanical samples (dummy FPGAs) are placed on test PCBs, and is followed by a 100% X-ray inspection. The FPGAs are 100% factory-tested. The FPGA logic is simulated individually as well as at the board level. The test plan presented below address the problems that escape detection in these processes.

Problems that arise from the algorithm definition may not be located if the same problem exists in the simulation software. Problems related to the communication with the other part of the DCT system will be revealed only at the system-level testing at SLAC.

2 Infrastructure

The testing will take place both at the production site (Harvard), and at the experiment site (SLAC). A test stand has been set up at each site.

2.1 Harvard Test Stand

The test stand at Harvard is built around a test board[2] controlled by a PC. Figure 1 shows the block diagram of the test board.

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[1] http://www.slac.stanford.edu/BFROOT/www/Detector/Trigger/upgrade/fdr/zpd/ZPDTestPlan.pdf

[2] Based on an amplifier chip tester developed for ATLAS muon system.

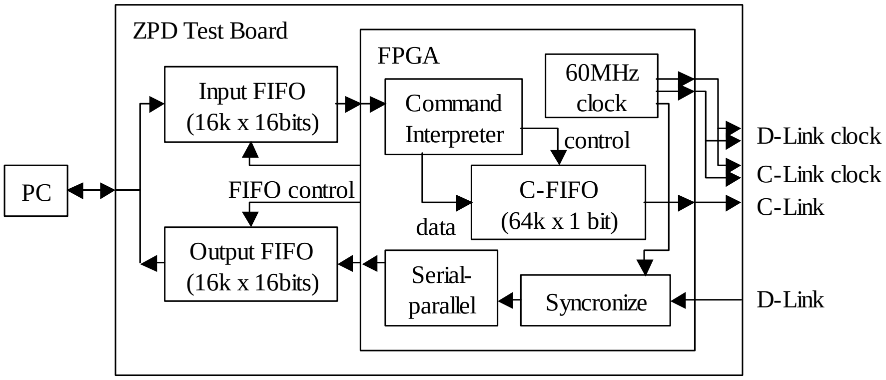

Figure 1: Block diagram of the ZPD test board at the Harvard test stand

The FIFOs on the test board enable it

- to send arbitrary bit sequences to the CLINK of a ZPD module, and
- to record the output from the DLINK.

Through this test board, the PC can communicate with the ZPD module using the BABAR Fast-Control Command (FCC) protocol.

The Harvard test stand has been used for debugging the prototype ZPD module. The system is capable of sending arbitrary combinations of all the FCC commands and interpreting the output. In addition, specialized programs for memory and algorithm tests have been written and used.

2.2 SLAC Test Stand

The test stand at SLAC is a standard BABAR DAQ test stand, located in the Dataflow Lab. Software based on the BABAR Online Calibration framework drives the system to perform various tests. In addition, a set of low-level test commands, issued at VxWorks prompt on the ROM, has been written to facilitate the hardware/firmware debugging.

3 Connectivity Tests

The ZPD module carries 8 FPGAs (1 Receiver/Driver, 6 Algorithm Engines, and 1 Decision Module) and little else. The FPGAs have large footprint, which is necessary to accommodate large numbers of connections using Ball Grid Arrays (BGAs). Ensuring the connectivity between the FPGAs therefore confirms much of the integrity of the PCB.

3.1 Boundary Scan

The connectivity on the PCB, as well as short circuits, can be detected with a boundary scan. Harvard has acquired a tool for the boundary scan, but has not used it during the testing of the prototype. The plan is to apply the boundary scan tool on the prototype during the period of PCB manufacturing in order to gain experience in time.

There remains a question if the boundary-scan technique is applicable for the MegaBus, a 75-bit wide LVDS bus that carry the TSF segment data to the Algorithm Engines. If the boundary scan does not work for the MegaBus, we need to have an alternative testing method to ensure the connectivity. Even if the MegaBus can be boundary-scanned, it is still useful to perform a dedicated test in which a large amount of pseudo data are transferred over the MegaBus at the expected speed (120 MHz) and higher. Such a test is possible by one of the two methods discussed below.

3.2 Memory-to-Memory Transfer Test

Each FPGA has diagnostic memories that record and playback the input and output data streams. The output memory of the Receiver/Driver can be loaded with various bit patterns, which are transmitted through the MegaBus and recorded in the Algorithm Engines input memory. These memories can be accessed via Fast Control interface so that a test program can check the data consistency.

This test method has the advantage of being simple and flexible. The data transfer over the Fast Control interface limits the speed to less than 10 Mbits/s, and probably significantly lower. This is at least 3 orders of magnitude slower than the capacity of the MegaBus, and makes it difficult to ensure that the bit-error rate is lower than what is permissible.

The prototype has been tested in this method at both sites, exhibiting no problems.

3.3 Pattern Generator Test

An alternative approach to the memory-to-memory test is to implement a simple pattern generator (e.g. an incremental counter or a rotating bit shifter) in the Receiver/Driver. The Algorithm Engines lock in to the pattern and look for errors. The error count are sent to the Decision Module via the 10-bit bus (which carries the fit results during normal operation). The Decision Module monitors the error counts and reports them through the front panel LEDs.

This method allows testing of the MegaBus at its maximum speed (~10 Gbits/s). A 24-hour test will ensure the integrity of the bus at the 10^{-15} level. The test should be attempted at higher-than-nominal clock rates to ensure the headroom.

The prototype has been tested in this method (at the nominal clock rate) at both sites and exhibited no problems up to ~10^{15} bits.

3.4 Interface Test

Another potential point of failure is the traces that run between the input/output FPGAs and the backplane connectors, and the connectors themselves. It is therefore important to test the communication between the ZPD module and the ZPDi card. This test is likely to take place at SLAC due to the availability of the ZPDi card.

There are 153 input signals and 6 output signals on the ZPD backplane connector. The inputs are 60 MHz and the outputs are 7.5 MHz.

The input signals can be tested using a special version of the ZPDi firmware that produces repetitive bit patterns. The receiver FPGA on the ZPD module is configured to recognize the pattern, and to report bit errors through the front panel LEDs. This method is similar to the pattern generator test of the Megabus discussed above, and can easily ensure the integrity of the input signals at the 10^{-15} level. Again, it is important for this test to be performed at higher-than-nominal clock rates.

Since there are only 6 output signals and they are slower, it suffices to generate bit patterns by loading the output diagnostic memory and playing it repeatedly, and to monitor them with a logic analyzer.

The prototype has been tested for both input and output signals with no problems.

4 Functionality Tests

Once the connectivity is established, the module is tested for its functionalities, i.e.

- The module must respond to all the Fast-Control Commands (FCC);
- All on-board memories must be read and written;
- The module must process input data and produce expected results;
- The module must capture the DAQ data upon Level-1 Accept, and send it in response to Read Event.

Software has been written, at both sites, to test the first 3 items and used to test the prototype. The last item is being implemented.

4.1 FCC Test

Given the number and the flexibility of the Fast-Control Commands, it is impossible to cover the entire input space of the FCCs in finite time. It is expected that failure of any FCC will be revealed in the later tests that require coordinated use of multiple FCCs. It is nevertheless important to ensure that the FCC interface is functioning properly, for example, by setting the internal status registers and reading them back.

4.2 Memory Test

There are many memory blocks on ZPD:

- Look-up tables that implement the ZPD algorithms,
- Diagnostic memories that record the data as they flow,
- DAQ memories for the event data.

All of them can be accessed through FCCs. Software has been written at both sites to test all the memories by writing random bit patterns and reading them back.

4.3 Algorithm Test

The algorithm can be tested using the diagnostic memories, which are distributed through the ZPD module as shown in Table 1.

Table 1 Diagnostic Memories on ZPD

Name	***Location***	***Contents***
Input memory	Decoder/Driver	Data sent over the Megabus
Megabus memory	Algorithm Engines	Data received from the Magabus
Finder memory	Algorithm Engines	Data sent from Finder to Fitter
Fitter memory	Algorithm Engines	Data sent over the Fit Result bus
Fit Result memory	Decision Module	Data received from the Fit Result bus
Output memory	Decision Module	Data sent to ZPDi

One can test the ZPD algorithm by loading any of the (upstream) diagnostic memories, playing it, reading back another (downstream) memory, and comparing the contents with the expectation from the simulation.

Software has been written on both sites to perform this test, and has been used on the prototype to debug the firmware.

4.4 DAQ Test

When a Level-1 Accept is issued, the ZPD module must capture the current data in one of the 4 event buffers. The data is later retrieved by a Read Event command.

This is one of the most difficult part of the testing, as it requires synchronization of multiple FCC commands, in particular the Level-1 Accept, and the known data pattern that is flowing through the module. The simplest solution requires loading a test pattern in the diagnostic memories, playing it, and sending Level-1 Accept after a known time interval. The software for this testing is being developed.

5 Readiness and Man Power

Much of the preparation for the testing has been done as a part of the prototype development. In particular, the testing infrastructure and most of the software are already available. Notable exceptions are:

- Tests with higher-than-nominal clock rates. This has not been done, but is easy to accomplish at the Harvard test stand by replacing the crystal. The SLAC test stand is believed to be capable of running at 62.5 MHz; this needs to be confirmed.
- The DAQ test software is under development at both sites.

The following personnel are available for the testing of the ZPD modules:

- Harvard test stand: G. Brandenburg, N. Felt.
- SLAC test stand: S. Bailey, M. Morii, E. Won.

In addition, we expect to have one graduate student (K. Chaisanguanthum) and one undergraduate student (K. Weil) at SLAC starting in June.