

ZPD Board Modifications

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This document summarizes the modifications to the ZPD PCB between the prototype and the final production version.

1 Overview

We have produced ZPD prototype modules in early 2002. Since then, we have identified a number of design and engineering issues that need to be addressed for the final production version. In particular, there was a bug in the PCB layout software that resulted in loss of power connections for some of the FPGAs. Although we have managed to fix this problem by adding jumpers, and the prototype did work, it is obvious that the PCB layout must be redone for the production version. We have therefore decided to take advantage of this iteration and fix other, mostly minor, issues at the same time. The issues we intend to address are summarized in the next section.

2 Board Modifications

2.1 Power Distribution

On the prototype board, many vias that were supposed to bring VCC to the FPGAs were found disconnected. The problem was traced to a bug in the PCB layout software. We worked around the problem by adding jumper wires on the backside of the board, and the prototype did function. Reliability consideration nevertheless demands that we redo the PCB layout.

2.2 Clock Input to FPGAs

The Xilinx Virtex-II family FPGAs have “global clock” (GCLK) pins that are specially designed for accepting clock signals. The timing from the GCLK pins to the digital clock manager (DCM) unit is guaranteed. On the prototype board, the 60 MHz clocks (cclk and dclk) are fed to the FPGAs through normal user I/O pins. As a result, the timing of the clock inside the FPGAs depends on the place-and-routing inside. This caused, for example, the phase of the DLINK output relative to the system clock to vary from one implementation of the firmware to another. We route the differential 60 MHz input clocks into dedicated clock pins on the production PCB.

2.3 FPGA Configuration Scheme

In order to configure the FPGAs on the prototype, we adopted a solution called System ACE MP. In this scheme, the firmware code is stored in a flash memory inside a small

hybrid LSI, which configures multiple FPGAs on power up. To update the firmware, one can download the new design into the flash memory through JTAG.

Although this solution offers fast, multi-FPGA configuration in a small (2.25 cm²) package, we found the technology immature. We encountered numerous problems our Xilinx field engineer could not diagnose. The support software was unstable, and downloading a full design took nearly an hour. We considered the latter particularly problematic because it would take a full shift to update the entire ZPD system of 8 modules.

Xilinx offers another solution called System ACE CF, in which the firmware code is stored in a Compact Flash (CF) memory. The system consists of a CF socket and a small controller chip. On power up, the controller reads the firmware file from the CF memory and configures the FPGAs via JTAG. Since CF memories and the PC adaptors are inexpensive and widely available, design update is extremely easy. One can copy the design file on a CF memory using any PC and replace it with the old one on the board. (The CF memories are hot swappable.) The controller recognizes the new design and reconfigures the FPGAs automatically.

To confirm the usability of the CF solution, we have developed a small add-on board for the ZPD module. The board carries a CF socket and a controller chip. With this board, we could configure the ZPD module from a CF memory. This proved to be so effortless that we have never gone back to the original MP solution. Although the CF solution is theoretically slower to configure the FPGAs, it takes only a few seconds for the full ZPD design.

There is, however, one outstanding issue related to the System ACE CF. When the design is updated, even though the controller recognizes the change, it often fails to reconfigure the FPGAs correctly. A hard reset (or a power cycle) is needed to ensure that the new firmware is properly downloaded. We believe that the problem is in the Xilinx software. If this problem is not resolved, we will have to push the reset button on the front panel every time we replace the CF memory. Note that the configuration from the CF memory works correctly with power cycling; no human intervention is necessary after a power interruption.

On the production board, we switch to the System ACE CF solution. The CF socket is placed near the top of the front panel, which needs to be reorganized to accommodate the socket. We also add a jumper field to make the front panel reset switch perform FPGA reset, System ACE controller reset, or both.

2.4 Minor Modifications

Additional minor modifications have been made:

- Better silkscreen labels.
- More dedicated signal test points.
- Added board serial number jumper field.

3 Final PCB Layout

The PCB layout for the production version is complete. It has been quadruple-checked by the layout technician, two engineers and a physicist. The final design is available online from the FDR documentation page.