ZPD Decision Module Algorithm Definition

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1 Overview

This document defines the algorithm implemented in the Decision Module of the Z P_T Discriminator (ZPD). The Decision Module receives inputs from 6 Algorithm Engines (AEs) at every CLK8 and determines whether they satisfied a set of programmable criteria that indicate the potential presence of a track from a physics event. At the end of each CLK4 cycle, the Decision Module produces an 8-bit output, each bit corresponding to one set of decision criteria being satisfied by at least 1 track candidate, and sends it to the Global Trigger (GLT).

2 I/O Definition

2.1 Inputs

Each of the 6 Algorithm Engines processes 2 seed segments per CLK4 cycle, producing as a result one fitted track per CLK8. Each fitted track is represented by 38 bits:

Quantity	***Bits***	***Unit***
z_0	8	cm
z_0 error	4	cm
track curvature	8	2^{-12}/cm
tan$l$	8	2^{-5}
segment map	10	

These data are time-multiplexed and transmitted over 12 point-to-point connections from each Algorithm Engine to the Decision Module.

CLK30	***MSB.....LSB***				
0			segment map		
1	z_0 error			curvature	
2					z_0
3					tan$l$

2.2 Outputs

An 8-bit output is reported at the end of each CLK4 to the GLT. Note that only 6 out of 8 bits are physically transported to the ZPDi card, and only 4 bits are accepted by the GLT. The extra bits are implemented so as to allow for future expansion.

3 Algorithm

The Decision Module supports up to 8 independently programmable decision algorithms. Each algorithm is applied to each fitted tracks, producing either 1 (TRUE) or 0 (FALSE). Mapping of the results (8 sets of criteria times 12 tracks) on the final 8-bit output must

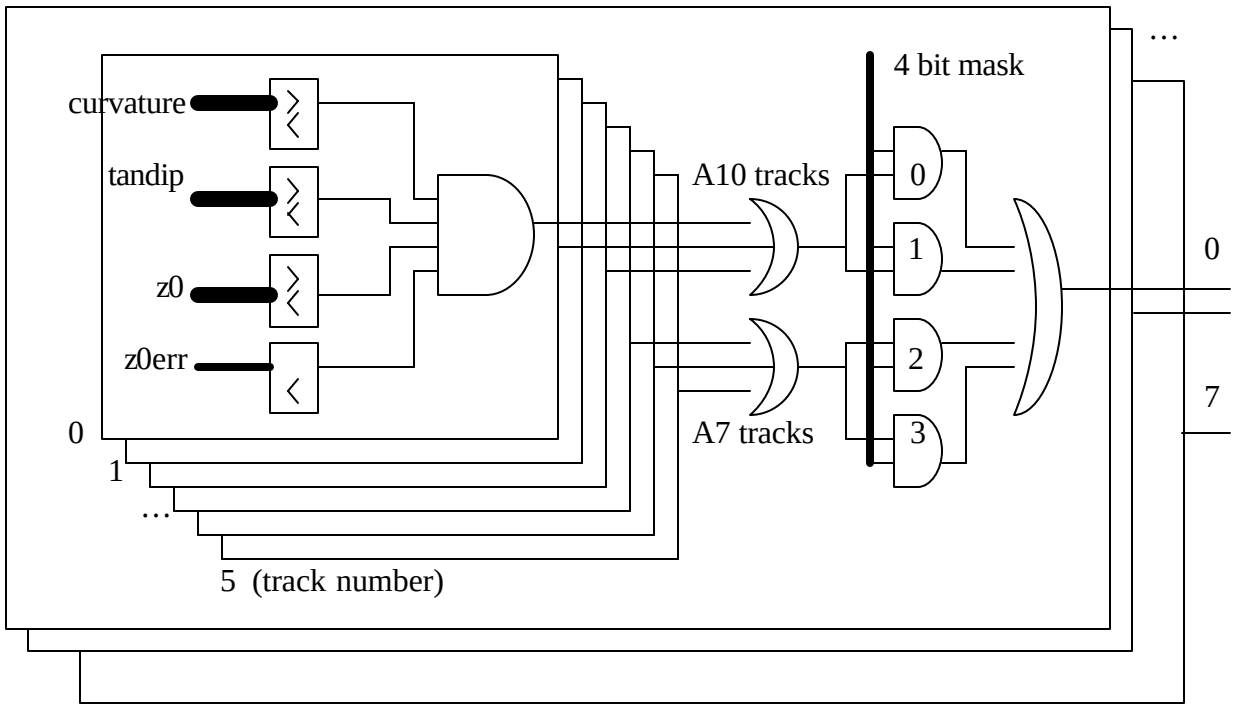
also be configurable. Ideally, we want a flexible and fast solution that does not require excessive amount of resources. A simple but functional solution is presented here.

3.1 Strawman Algorithm

1. For each track candidate, the curvature, tan$l$, z_0 and z_0 error are compared with the maximum/minimum values in 8 sets of look-up tables (LUTs). (For z0 error, only the maximum value is considered.)
2. The output from the comparison are ANDed. This produces 8-but output for each track.
3. An OR of 3 tracks that came from one superlayer (7 or 10) of one 1/16 sector is formed. This produces 4 times 8-bit outputs.
4. For each bit, a set of superlayer/sector combinations are ORed, and sent to output.

The block diagram and the LUT organization are given below. Although this design allows only "box" cuts on the relevant parameters, it does offer considerable flexibility in mapping of the output bits. Consider, for example:

- Bits 0 and 1 use tight cut on z_0 and moderate cut on p_T. Bit 0/1 are mapped for the odd/even sector. We can consider them as the "Z" trigger.
- Bit 2 uses loose cut on z_0 and tighter cut on p_T. Both sectors are accepted. We can consider it as the "low multiplicity" trigger.
- Bit 3 uses a tight cut on p_T and no cut on z_0. Both sectors are accepted. We can consider this as replacing the PTD.



(Block Diagram of Strawman's Decision Logic)

Memory Map (0x100 – 0x8f0)

Decision bit: a (7-0)
Seed number: b (1-0) 0: for A10, 1: for A7 seed

Address	Contents	size (bit)
0(a+1)b0	ρ min	8
0(a+1)b1	ρ max	8
0 (a+1)b2	tanλ min	8
0(a+1)b3	tanλ max	8
0(a+1)b4	z_0 min	8
0(a+1)b5	z_0 max	8
0(a+1)b6	$z_0$err max	4
spare…		
0(a+1)f0	4 bit mask	4 (LSB: top bit, labeled as 0 in the figure)

(LUT's for Strawman's Decision Logic)