

Interface Board Production Plan

Version 0.0

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1 Changes to prototypes for production

The L1 DCT upgrade include 3 types of new interface boards TSFi, ZPDi, GLTi. Following the prototype testing, there were some design issues detected on each board which will result in modifications for the production:

ZPDi:

- Original ZPDi did not allow pursuit of timing alignment between data from the 9 TSFs in ZPDi and the issue of dealing with missing data (happen all the time during tests with not all cables connected). New scheme to deal with both issues is to use two of the spare lines to ZPD backplane to formally route clk60 from ZPD as LVDS pairs and choose appropriate pins on the switch FPGAs to allow clean access to global buffers in the FPGAs for good clock distribution. Prototype used a single ended signal line for the ZPD clock and non optimal FPGA pin. Modification include addition of an LVDS receiver and more careful routing of the clock lines to new FPGA pins.
- Prototype ZPDi used two rather bulky DC-DC convertors to supply 3.3V to the 3 switch FPGAs. This may be replaced by simpler regulators.
- The LVDS channel link connectors on prototype are held to the board by the soldering without additional mechanical mounting support. It may be more prudent to use an alternative part with mechanical mounting holes on the side to secure the sockets. This needs substantial work to move active components to clear the space for adding mounting holes.
- Two LED signals need terminating resistors added.
- Some connector label prints could be moved into more visible locations and correcting one label problem.
- Some frame bit signal pin out are swapped compared to original spec, but this can be corrected by renaming schematic and firmware signal names without any actual hardware board modification.

TSFi:

- One pinout mistake on prototype needs correction to move signal to another pin.
- Mechanical mounting holes for Finisar receiver are too small.
- The crystal oscillator socket footprint is for old 8 pin crystals. Need to change to 4 pin footprint for modern parts.
- Similar concern as ZPDi for the LVDS channel link connector mechanical mounting could be strengthened.
- Connector label prints could be improved at a few places.

GLTi:

- ZPD LVDS signal receivers are missing terminating resistors. This could be fixed by adding terminating resistors on the ZPDi side also (which may be more beneficial as the GLTi is already very crowded).
- As the first interface prototype board built, a Spartan XCS40 FPGA was picked and only found out later that the Xilinx software tools have dropped support in new versions for this FPGA. Should replace it with a later model, and perhaps slightly faster speed to allow more flexible switching between new and old system (old system PTD delay unfortunately maxed out unnecessarily, leaving very little room to signal switching).
- Some connector label prints need to be added.

In addition, the front-panels designs need to be completed for at least ZPDi and TSFi to make sure there are no mechanical conflicts.

2 Production Plan and Schedule

The PCB fabrication can proceed with many local companies who can typically deliver on 10 day scale. The board component assembly was done in house for the prototypes, while production will be using external vendors. There is no attempt to get quote yet for the assembly vendors, but a reasonable estimate for delivery time is 3 weeks. For a targeted commissioning effort starting mid June for two weeks before the end of the run, with a 1/8 wedge of the detector, the required interface boards are 2-6 TSFi's, 1-3 ZPDi's and 1 GLTi. The prototype GLTi's and ZPDi's are probably even sufficient to serve that purpose. However, to avoid making any further loading of prototype boards, we need to have a few production TSFi boards. Allowing 5 weeks of PCB production and assembly and 1-2 weeks of Lab. testing, the TSFi PCB production need to start by Apr/28. This is still possible provided the TSF prototype input/output memories are functional by the time of the FDR to allow all TSFi related interface tests to proceed. During the prototyping phase, components with long lead times (e.g. PECL driver/receivers) were identified and orders for production are already placed.

3 Manpower/Cost

3.1 Manpower

Personnels involved in the interface board design, production and testing:

| | | |
|---------------------------|--------|---|
| Su Dong | SLAC | Coordination, design and testing |
| Jeff Olsen | SLAC | Engineering design, firmware, layout |
| Xuedong Chai | U Iowa | Firmware, testing and software |
| Sangjoon Lee ¹ | U Iowa | Firmware and testing |
| Chuck Yee | SLAC | Fabrication |
| Mark Freytag | SLAC | Infrastructure support, cabling, panels |

Table 1: Interface board design, production and testing manpower.

3.2 Cost

At the time of the CDR, the interface cost underestimated 4 major sources:

- The engineering effort for designing all 3 boards is considerably higher than the original estimate of 0.3 FTE.
- The board assembly was unsure to be in house or external and only a very small amount was quoted per board which was clearly an under estimate.
- There was no estimate for the cabling cost. The stringent cable spec required for the LVDS channel links propelled the conservative choice of the micro-coax cables, which is very expensive at \sim \$150 per piece (and we need 72+8).
- The original hope was one round of production PCB only without change from prototype, but actual prototype have various problems which are clearly beneficial to correct for the production version. The PCBs therefore need to be made again.

At the time of the Capital Equipment Project (CEP) budget setup in 2002, the first three items were already largely corrected, while the PCB refabrication is a late addition. Most of the costs are now known for the interface boards, but there are still uncertainties on a few main sources. The major uncertainty is the assembly cost. An estimate of \sim 200\$/board, including component loading and a front-panel fabrication, is used to estimate the total. The TSFi PCB prototype was priced at \$275/board for 4 boards and the 30 board production should have significantly lower cost per board. The best estimate are summarized in Tables 2 and 3.

| | | Current | CDR |
|------|------------|--------------|-------|
| TSFi | PCB | <i>\$200</i> | \$200 |
| | components | <i>\$475</i> | \$470 |
| ZPDi | PCB | \$175 | \$200 |
| | components | <i>\$390</i> | \$460 |
| GLTi | PCB | <i>\$406</i> | \$200 |
| | components | <i>\$420</i> | \$160 |

Table 2: Per board cost comparison with CDR estimate. Current items with *slanted numbers* are still rough estimates.

| | | No. of boards | Current Estimate | CDR sum | CEP budget |
|-------------|------------|---------------|------------------|----------|------------|
| TSFi | PCB | 30 | \$6000 | \$6000 | |
| | components | 32 | \$15200 | \$14100 | |
| | assembly | 28 | <i>\$6000</i> | \$750 | |
| ZPDi | PCB | 12 | \$2100 | \$2200 | |
| | components | 15 | \$5850 | \$5060 | |
| | assembly | 12 | <i>\$2400</i> | \$275 | |
| GLTi | PCB | 4 | \$1600 | \$600 | |
| | components | 5 | \$2110 | \$300 | |
| | assembly | 3 | <i>\$600</i> | \$75 | |
| LVDS cable | | 80 | \$12000 | - | \$12300 |
| Prototyping | | | \$8000 | - | - |
| M & S Total | | | \$61,860 | \$29,540 | \$51,900 |
| ED & I | | | <i>~0.7 FTE</i> | 0.25 FTE | 0.56 FTE |

Table 3: Overall cost comparison with CDR estimate. Current items with *slanted numbers* are still rough estimates.