

L1 Drift-Chamber Trigger Upgrade Interface Specification

Version 1.0

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1 Introduction

The L1 DCT system receives wire hit pattern input data from the drift chamber via GLINK fibers at 267ns (clock-4) intervals. The data is first processed by the TSF to reconstruct track segments. At the end phase of the TSF processing, segment hits are Ored to determine which supercell (1/32th of azimuth in each superlayer) have hits and this ‘coarse ϕ ’ data is sent to the BLT. Segments with ‘fine ϕ ’ information according to the lookup table calibration are used by the PTD in the present system and will be used by the ZPD in the upgrade system. The BLT output 2 16-bit ϕ -maps (A and B for long and short tracks) to the GLT every 134 ns. The current PTD output 2 bits per PTD to assemble a 16-bit ϕ -map for the A’ at the GLT every 267 ns. Each of the 8 new ZPD will output 4 bits per board to assemble 32 bits of information at the GLT each 134 ns.

The DCT and GLT modules are all housed in 9U VME trigger frontend crates with a custom built backplane [1] for the L1 trigger boards. The J1 and J2 connectors are 3×32 and 5×32, respectively, containing mostly single slot straight through user pins together with some common ground and power pins. All external I/O signals are communicated through the backplane to the DCT boards. Each DCT board has a corresponding back-of-crate 6U VME auxiliary board as the interface for external I/O. For example, each TSF has a TSFi interface board for receiving input data from DCH, passing data between neighbor TSFs and output signals to BLT, PTD/ZPD. The J3 connector is dedicated to fast control communications to the external world, using the DIRC backplane design. The DIRC Crate Controller (DCC) is located at slot-5 for each of these crates to control the communication between ROMs via GLINK fibers and the 60 MHz serial C/D links to individual modules in the frontend crates.

A summary of the interface decisions:

Front-end Crates We have decided to retain the current front-end crate backplanes for the new system and continue to follow the *BABAR* common standard of passing external signals via backplane only.

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TSFi A full set of TSFi need to be rebuilt mainly for the new TSF to ZPD data path with a much higher data volume compared to the previous TSF to PTD data. Each TSF transmits same copy of data to 3 ZPDs, containing information on 21 (18) segments for TSF_x (TSF_y).

BLTi Keep existing board.

ZPDi These are new set of interface boards for receiving TSF data and feeding the ZPDs. It will transport 6 bit output from each ZPD to the GLT, while initial design will only use 4 bits at GLT.

GLTi Keep the number of inputs to GLT as before to continue using existing GLT. The ZPDs will contribute 2 signals of 16 bits each to the GLT. One signal will occupy the current A' signal slot. The other ZPD signal has to displace the current EMT X signal. This requires rebuilding the GLTi, but with simple connector addition and capability to switch between old and new inputs.

A few comments regarding to the decision on the front end crates: Retaining the old custom made backplane maximizes the sharable resources between the test and production systems. An option of keeping the back of crate system intact, but using special front panel connections for TSF to ZPD data transport, was briefly considered and dismissed. This option does not appear to have extra reliability advantages and the main drawback is the front panel connectors may need to be repeatedly connected and disconnected for any module replacements or firmware upgrades, which present a significant risk and all experience with present systems in *BABAR* having this type of arrangements are not good. The amount of signals to be transmitted from TSF to ZPD can still fit in to the available user pins, although the pin count is very tight at the ZPD backplane. It was also discussed whether we need to build a new backplane for the ZPD. Given that the scheme we decided on is a reasonable balance point for signal volume and algorithm performance trade off, there is no longer any advantage in performance gain from increasing input signals compared to the complication of both the interface and the ZPD internal resources to store the extra inputs. For all the new upgraded boards (TSF, ZPD), it is most likely that the devices they use typically require lower DC voltages (e.g., the Xilinx Virtex-II series uses 1.5V). Using the existing crates with 5V supplies means that these new boards will need on board DC-DC converters or regulators.

2 The TSF to ZPD Data Requirement Study

2.1 TSF segment selection

The TSF fine- ϕ data was previously only used by the PTD, and one 'best' segment per supercell ($1/32^{nd}$ of 2π) from only the axial superlayer was chosen for the PTD. This was sufficient for the simple p_T envelope algorithm of the PTD. With the ambitious goal of full 3D track fitting in the ZPD, and knowing the single hit resolution from the TSF is just adequate, we need to promote as many as possible real track segments.

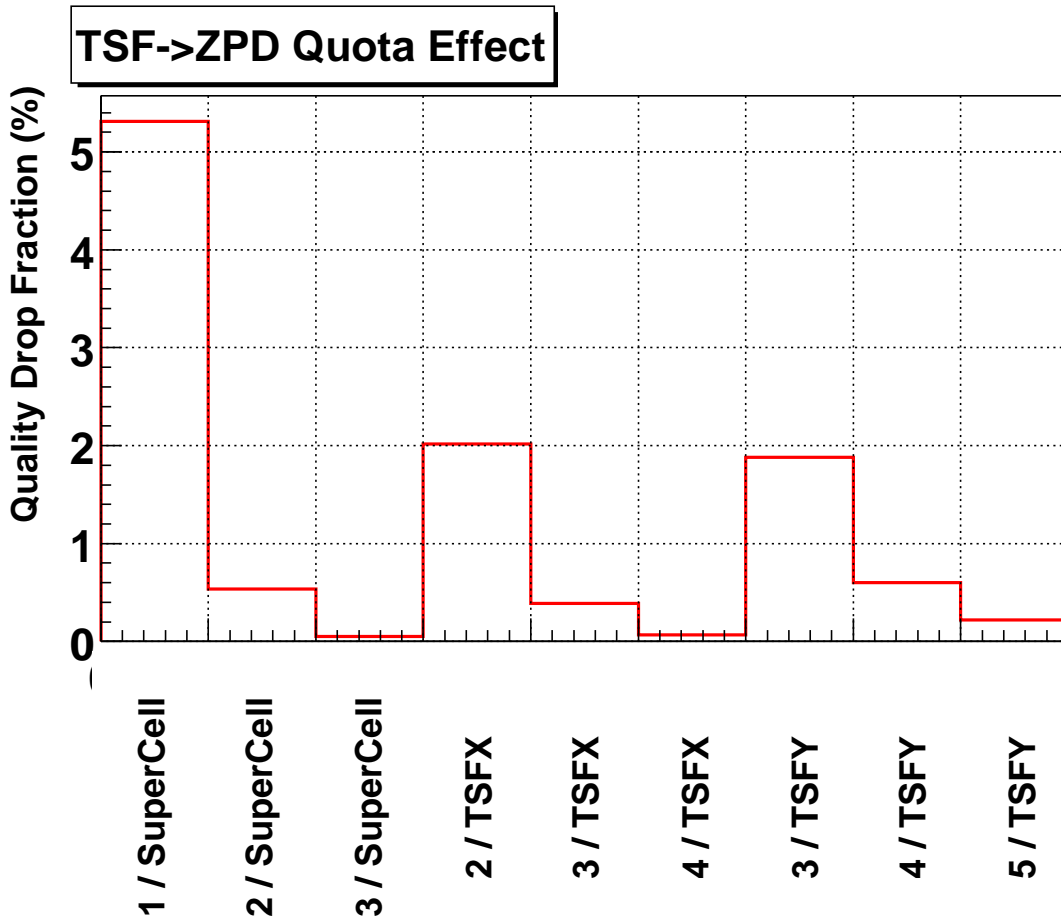


Figure 1: The TSF to ZPD selection segment quality loss in hadronic events.

A series of studies [2] eventually concluded that 3 best segments from each sector of $2\pi/16$ (full ϕ span of a TSFX, half ϕ span of a TSFY) is the best compromise. To select the best TSF segments, only segments with fine- ϕ data (ϕ error $< 5\text{mm}$) are allowed. A priority scheme is made to define a rank for each segment based on its hit pattern and weight (calibrated resolution category). This rank value is implementable as a simple 4 bit lookup table for each segment. The selection simply chooses first N segments with the highest rank from a ϕ sector from each superlayer. We have considered the quota N imposed on ϕ -sectors being a supercell ($2\pi/32$), TSFX width ($2\pi/16$), and TSFY width ($2\pi/8$). We examined the quality of the selection based on the TSF segment hit wire matching to the offline reco track hits. A segment with majority of its hit wires being hit wires on a Reco track, the segment is labeled as a ‘good’ segment for the track. Figure 1 shows the fraction of tracks originally having a good segment at a superlayer, but ended up with a bad segment or no segment after the selection with the TSF to ZPD quota imposed. This test is done for various selection schemes on hadronic events. Among the different schemes, the original 1/supercell scheme for the TSF to PTD is clearly rather inefficient. The 3/TSFX scheme is in fact performing slightly better than the 2/supercell scheme although the latter will

effectively send 4/TSFY. This can be understood as giving the local quota to the widest range available is always better than constraining the quota to small regions for a fixed total promotion quota for the whole detector. However, in the case of the TSFY, although one would prefer the 5/TSFY scheme, it introduces a hardware asymmetry between TSFX and TSFY which would complicate the TSF implementation. Too wide a ϕ sector would also cost extra resources in the ZPD pattern recognition stage to make the seed ϕ correction. For these practical reasons, the TSFY segment selection is also chosen to be 3 per half TSFY.

Another possible improvement was to suppress segments in neighboring cells with the hope that the freed quota from this can preserve some isolated segments which might have got lost. However, tests indicate that the gain from this is diminished by the more often loss of genuine neighbor segments from different tracks. The neighbor segment comparison would also complicate the selection logic in TSF.

2.2 ZPD ϕ coverage

The PTD was limited to work on track with $p_T > \sim 500$ MeV/c using a not so wide envelope, taking data from 4 TSFX and 2 TSFY. Given the more generic functionality desired from the ZPD, it certainly need to be able to find tracks at much lower momentum. A kinematic model study [3] indicates that the efficiency for finding 1 Z track near IP can already be affected for some rare B decays and τ events, even for a rather low $p_T > 250$ MeV requirement. An ability to reach 200 MeV/c is quite desirable. However, a lowered p_T reach implies TSF inputs from wider ϕ region. A detailed study of the ϕ span of the TSF input segments to the ZPD is summarized in Figure 2. The input range certainly needs to be expanded to 6 TSFX and 3 TSFY. The tracks with their A10/A7 near the boundary of the central region may require data from two TSFX apart. The stereo stagger effect causes a large variation from layer to layer, as the wires are grouped together in one TSF based on the backward endplate wire locations. The ϕ shift limits are calculated only for tracks originate from the IP, which limits the ranges of z for inner superlayers. Allowing the full length of the DCH for inner layers would result in even larger staggers. This study shows that it is not possible to reach much below 250 MeV/c for the A10 seed, primarily because the U2 layer would start to need data even beyond the 9 TSF ensemble. On the other hand, the A7 seed can consistently cover down to 200 MeV/c.

With the ϕ span expanded to 9 TSFs and 3 segments per $2\pi/16$ for all 10 superlayers, the mount of data arriving at the ZPD is a factor of ~ 5 more than the old PTD inputs. This large amount of inputs turns out to be one of the major challenges for even the ZPD internal logic. With a simple format of 1 pin/cable carrying one segment of data, the full 9 TSF data inputs would amount to a total of 180 segments. The ZPD backplane unfortunately only has 178 user pins, of which 9 are used for framing and 4 to 8 are to be used for the outputs to the GLT. Fortunately, Figure 2 shows that many of the outermost $2\pi/16$ sectors on different layers are outside the p_T coverage envelope and therefore unneeded. As long as the segments arrive on one segment per pin, it is easy to mask out a group 3 from a sector. There are actually 12 groups of 3 can be masked out to reduce the total input segments to 144, which is now very much manageable for the backplane pin allocation.

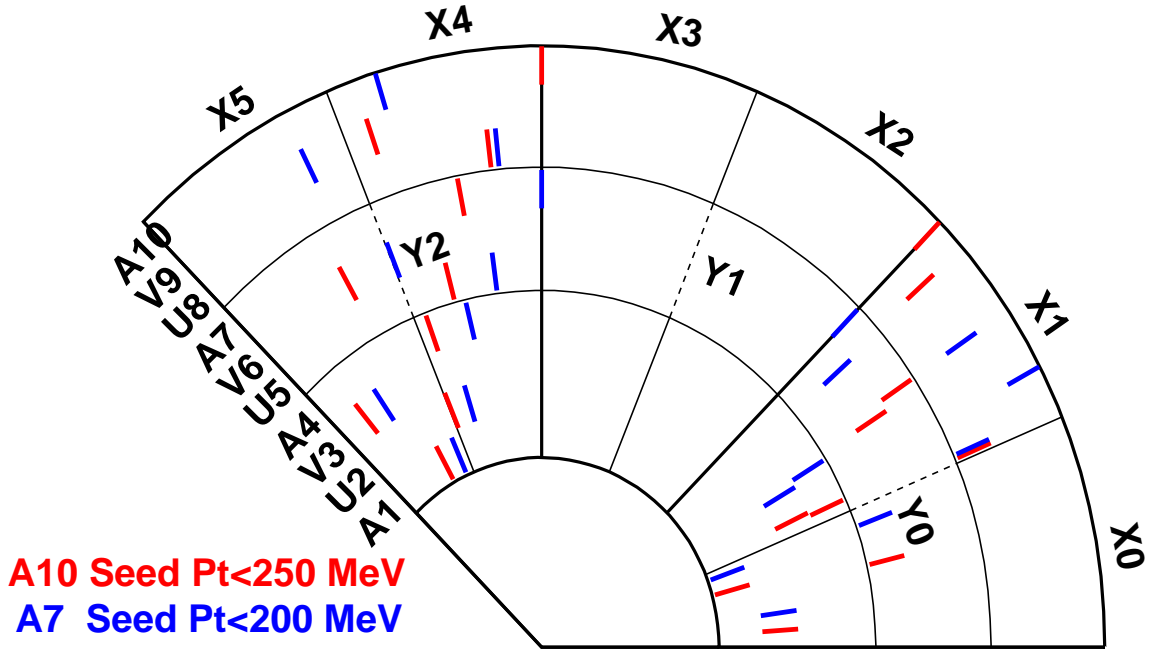


Figure 2: The TSF to ZPD input ϕ map. The ZPD is processing seeds from the central X2, X3, Y1 region. Also indicated are the minimum and maximum ϕ position where neighbor TSF data are needed to cover the p_T range indicated.

3 The Interface boards

3.1 TSFi

Some the basic features for the new TSFi:

- The DCH data receiving path (FINISAR+GLINK decoder) will remain as before, although the GLINK decoder part will be a modern version.
- The BLT data path will remain identical to before.
- The TSF neighbor data paths will also remain as before.
- The PTD data path will be modified to ship fine- ϕ data which will first be transmitted through backplane as differential LVDS at 60 MHz and then send to new ZPDs via LVDS channel link. Same copy of data will be fanout to 3 ZPDs.

The new TSF data format for the ZPD are listed in Figure 3. The TSF data for the ZPD will be sent via LVDS through the TSF backplane at 60 MHz to the TSFi. Since there are up to 21 segments in a TSFx plus the framing bit, we can use the National DS90CR287

LVDS transmitter which can group up to 28 inputs and send the signals to the ZPD. There should be 3 such transmitters to send the same data to 3 separate ZPDs. The clean fanout of the 3 channels of output data can use a small FPGA such as Xilinx Spartan-II XC2S150 to ease the timing alignment. This also has the advantage of allowing test patterns to be sent to ZPD for improved testability.

3.2 ZPD_i

The ZPD_i receives data via LVDS from 9 TSFs. The LVDS receiver can be the National DS90CR288 LVDS receiver to match the TSF transmission. The output TTL signals will first go through a set of FPGAs for masking out the unneeded outer neighbor segments. This masking can be done with 3 small FPGAs, such as Xilinx Spartan-II XC2S150, per ZPD_i. The masked signals will then go through the ZPD backplane to the ZPD at 60 MHz, single ended. The switch FPGAs again can provide pattern test capabilities through backplane to the ZPD. The output from the ZPD to GLT will be differential LVDS.

3.3 GLT_i

To make the transition between new and old systems easier, as will be needed in the parallel commissioning tests, the new GLT_i needs to be easily switchable between running the old and new systems. This can be achieved by allowing the cables from both old and new systems connected to GLT_i at all times and use a small FPGA to switch between ZPD signals and PTD+EMTX signals. Therefore switching between new and old systems can be simply changing a dip switch or replacing an FPGA PROM.

References

- [1] The backplane pinout can be found at the CDR backup material list:
<http://www.slac.stanford.edu/BFROOT/www/Detector/Trigger/upgrade/docs/interface/trg-backplane-pins.ps>
- [2] The track segment selection studies can be found at:
<http://babar-hn.slac.stanford.edu:5090/HyperNews/get/trignews/104.html>
<http://babar-hn.slac.stanford.edu:5090/HyperNews/get/trignews/104/1.html>
<http://babar-hn.slac.stanford.edu:5090/HyperNews/get/trignews/128.html>
- [3] <http://www.slac.stanford.edu/BFROOT/www/Detector/Trigger/upgrade/meeting-010718/schwanke/schwanke.html>

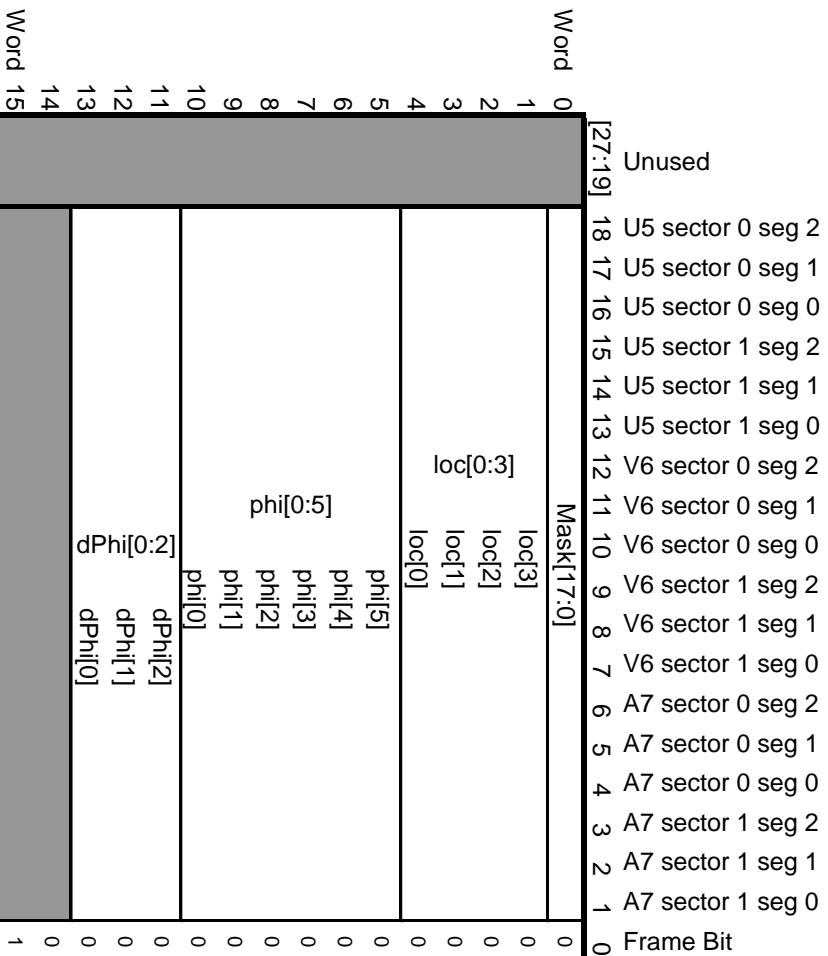
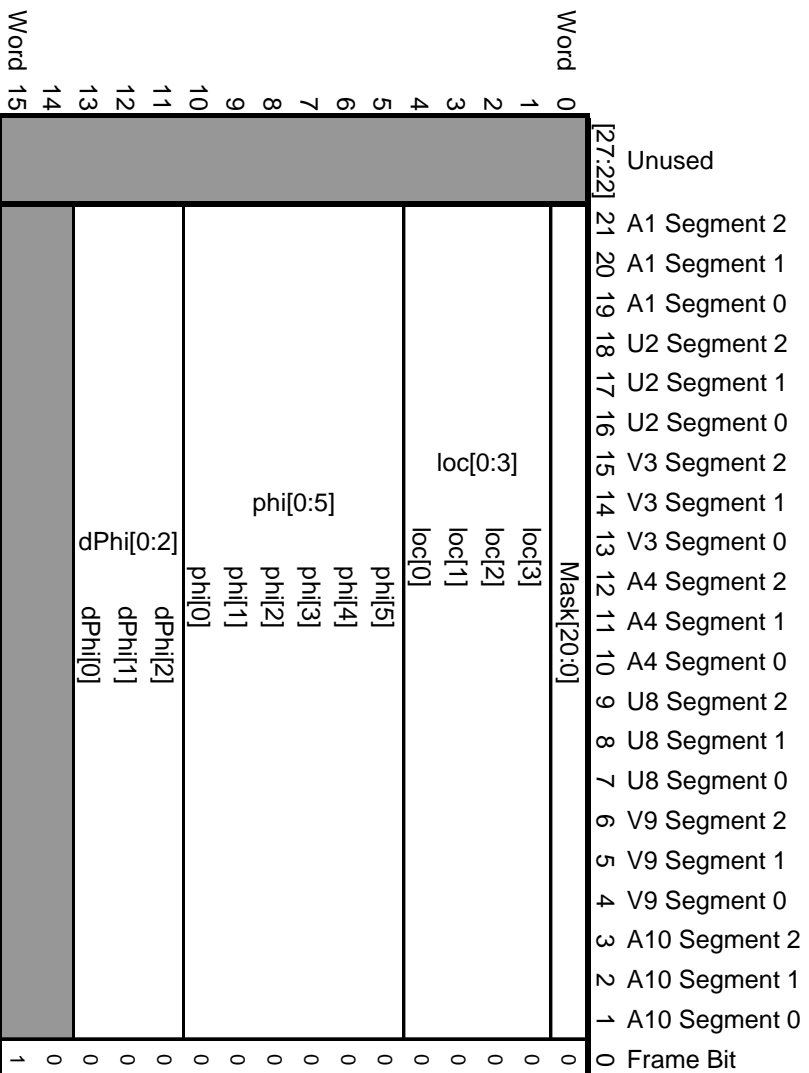


Figure 3: The TSFx/TSFy to ZPPD data format.