

L1 DCT Upgrade Interface Test Plan

Version 0.0

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The L1 DCT upgrade include 3 types of new interface boards TSFi, ZPDi, GLTi. The production testing for these interface boards essentially consist of various parts of overall system tests for validating not only the interface boards themselves, but also the cables, backplane connections, and I/O part of the various DCT boards. This document will first describe the procedure of a few main system tests which will be used to validate different aspects of different boards, and then followed by the individual interface board test procedures.

1 Main System Test Procedures

1.1 DCH-DCT Track Pattern Calibration

This has been a major facility for testing the combined DCH-DCT system which has been used at both IR2 and teststand to validate DCH frontend electronics and all boards involved in the DCT/GLT chain. The test is driven from the DCH calibration framework by pulsing the DCH frontend electronics and taking joint DCH and DCT DAQ data logged into XTC files. A track like pattern is created and slowly rotated around ϕ to make sure all DCH wires are pulsed in the process. The L3 event displays is typically used to inspect the DCH and TSF data overlaid together for hit matching.

This calibration is also available at the trigger Lab. in Central Lab. where a master crate delivers global timing controls to a TSF test crate at the trigger Lab. and the DCHproto test crate in the Central Lab. Annex. The DCHproto system contains a full $1/8 \phi$ -wedge instrumented with DIOMs and TIOMs (region covering $2 \text{ TSF}_x + 1 \text{ TSF}_y$) and the long trigger data fibers (similar length to IR2) connecting DCHproto to the trigger DCT crate TSFi inputs in the trigger Lab. Many thanks to Mike Kelsey and Karl Bouldin for their enthusiastic support of the system and effort in expanding the DCH calibration capabilities to allow more variety of such tests.

The DCH pulsing pattern is regular and can be used to derive an expect data pattern in the TSF event by event. However, a more robust test which doesn't even need the detailed knowledge of the DCH pattern can be done by placing a new TSF and an old TSF side by side, fed by data from the same DCH TIOM fiber (using a fiber splitter like in the real IR commissioning setup). Knowing the old TSF/TSFi should be working correctly already, the data received by the new TSF can be compared to the same data in the old TSF to validate the whole chain of DCH data receiving from TSFi Finisar to crate backplane and TSF input formatter. Once the new TSF DAQ is fully functional, the test can continue into the TSF algorithm output of TSF segments. Before that, one can still perform this test by reading

out the TSF input diagnostic memory recording the input pattern. The synchronization of the DCH pulsing and the TSF input memory recording through the playback fast control command is already incorporated into the DCH calibration sequence by Mike Kelsey. The whole calibration procedure still needs to run in the DAQ mode, and the new TSF can be setup to return dummy DAQ data initially for this test. The data logged will be analysed with a standalone test program to make bitwise comparisons between old and new TSFs.

1.2 Diagnostic Memory Playback Tests

Test patterns can be loaded into the output memories of an upstream board e.g. TSF and using the synchronized single shot playback to transmit the data through the interface boards, cables and backplanes and record the data in the input memory of a down stream board e.g. ZPD. The recorded pattern can be analysed on the fly in the ROM compared to expectation derived from the input pattern upstream. This general playback test using the calibration framework is also used for board internal algorithm tests from input to output and the software utility is already in place. These tests can always be done by placing the source and receiving boards in the same crate to synchronize control with one ROM, thanks to the backplane compatibility we retained for all old/new DCT/GLT boards.

The test patterns can be channel data = channel numbers to test connections, or walking '1's to systematically scan signal lines and checking cross talks. Examples of such tests include TSF→TSFi→ZPDi→ZPD, TSF→TSFi→TSFi→TSF neighbor data, ZPD→ZPDi→GLTi→GLT, or even GLT front-panel trigger-out →GLTi→GLT self-looping test.

1.3 Interface Firmware Pattern Tests

The introduction of the small FPGAs on the TSFi and ZPDi is in part to improve the testability. Test patterns are programmed into the firmware which can be activated with a mode switch or swapping a prom. The diagnostic memory pattern playback tests typically involve a long interface chain with two types of trigger boards and two types of interface boards. The firmware pattern test is a more isolated test between the main board and its interface board through the backplane. This is more convenient to conduct especially when not all boards for diagnostic memory pattern playback tests are available and very useful to isolate problems in case of failures in the playback tests. Unlike the playback test which is synchronized between the source and receiver, the firmware pattern tests need to look for test patterns at receiver with random timing offsets.

2 Interface Board Validation Procedures

Many of these tests need to be performed with many different components involved. For the test of a specific interface board, the other boards involved in the test need to be known functional, while each type of interface board needs to identify a standard working board to be used for testing other boards. The same principle also applies to the main trigger boards involved.

Because of the various combinations of boards involved in different tests, it is important to have good bookkeeping to avoid confusions. Given the issue of availability of all the boards needed for testing, the most efficient testing pattern may well be to perform a particular test for a number of production boards one by one, only substituting the board to be tested each time, rather than performing all different tests for one board before moving on to the next board. This will certainly need good tracking of test records of all boards simultaneously. A simple online test database (may be even just some plain text files) can be used to track the status of each production board:

- Board type and identification
- Firmware version, hardware modifications (if any)
- Known problems
- Checklist of tests performed on it. Each test needs its internal checklist, especially which other boards were involved in the tests.

This could be an extension of the existing Oracle hardware inventory database, but needs to check the capability of storing test checklists, archive of multiple test results etc.

2.1 TSFi tests

- Visual inspection for component loading and power up.
- DCH-DCT track pattern calibrations test for DCH data reception.
- TSF neighbor data test with a pair of TSFs and TSFis running diagnostic memory playback between each other.
- TSF→TSFi→BLTi→BLT memory playback test to qualify the BLT data path.
- TSFi firmware pattern test playing to ZPD to validate LVDS transmission of the ZPD data from TSFi to ZPDi.
- Full TSF to ZPD diagnostic memory playback test to conclude the whole ZPD path, particularly covering the TSF to TSFi backplane transmission and TSFi fanout FPGA timing not tested in the test above.
- Slow monitoring functionality tests. Details still to be defined. Can use a manual switch card to select monitoring channels and measuring output SV voltage by a Voltmeter. If the canbus monitoring is not very difficult to setup, it will be considered also.

2.2 ZPDi tests

- Visual inspection for component loading and power up.
- DCH-DCT track pattern calibrations test for DCH data reception.
- TSF neighbor data test with a pair of TSFs and TSFis running diagnostic memory playback between each other.
- TSF→TSFi→BLTi→BLT memory playback test to qualify the BLT data path.
- TSFi firmware pattern test playing to ZPD to validate LVDS transmission of the ZPD data from TSFi to ZPDi.
- Full TSF to ZPD diagnostic memory playback test to conclude the whole ZPD path, particularly covering the TSF to TSFi backplane transmission and TSFi fanout FPGA timing not tested in the test above.
- Slow monitoring functionality tests. Details still to be defined. Can use a manual switch card to select monitoring channels and measuring output SV voltage by a Voltmeter. If the canbus monitoring is not very difficult to setup, it will be considered also.

2.3 ZPDi tests

- Visual inspection for component loading and power up.
- ZPDi firmware pattern test playing to ZPD to validate ZPD crate backplane data transmission to ZPD.
- TSFi firmware pattern test playing to ZPD to validate LVDS channel link reception of TSF data. This test probably normally only has one TSFi available so that need to rotate the 3 channels to cover all 9 channels to be tested. Use the continuous playing pattern to do scope probing of frame bit timing skews between the 9 TSF channels.
- Full TSF to ZPD diagnostic memory playback test to conclude the whole ZPD path. May need to rotate 3 channels if only has one TSFi.
- ZPD→ZPDi→GLTi→GLT diagnostic memory playback test.

2.4 GLTi tests

- Visual inspection for component loading and power up.
- Scope check of GLTi Clock8 output to IFR trigger.

- GLT self-looping trigger out to GLTi input diagnostic memory playback tests. The GLTi receives data from all subsystems and it is too cumbersome to validate each input with a real subsystem component input. We will use a facility of original GLTi tests which take the 24bit GLT trigger line output controlled by output memory playback to split that into many channels with proper terminations and connectors fit into BLT/PTD/ZPD/EMT/IFT input sockets to make the memory playback tests. Although the cables and sockets need to be rotated several times to cover all types of signals.
- BLT→BLTi→GLTi→GLT diagnostic memory playback. This can be an optional addition to test the BLT→GLT timing as the GLT self looping test signal phasing is slightly different.
- PTD→PTDi→GLTi→GLT diagnostic memory playback. This can be an optional addition for just one or two GLTis to be used in parallel commissioning for both old and new systems.
- EMT→GLTi→GLT diagnostic memory playback. This is in principle possible, but the software implementations have not been investigated. The EMT sends data at down edge of clock8 which is a very safe timing option compared to the old DCT boards, so that the first test with GLT self-looping is probably a sufficient substitute for this test.
- Given the multiple inputs to the GLTi, a more comprehensive overall test is in fact real cosmic tests at IR2 which we will seek opportunities to try.