

ZPD Event Data Format¹

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Masahiro Morii, Eunil Won

1 Overview

The ZPD system processes the “snapshot” of the DCH, arriving in the form of TSF segments, at every CLK4. Each CLK4 cycle is considered independently. The event data (or “DAQ data”) is produced every CLK4 and recorded in the DAQ memories. The DAQ memories consist of circular buffers, that hold the data for the Level 1 Trigger latency, and 4 sets of event buffers to which the data is copied from the circular buffers upon Level 1 Accept. The circular buffers are 64 words long, allowing for the maximum latency of 17.2 μ s. (The BABAR DAQ system requires this to be at least 12 μ s.) The length of each event buffer is 8 words, or 2.2 μ s.

2 DAQ Memories

2.1 Input DAQ Memory

The input to each ZPD module contains up to 153 TSF segments. The data for each segment start with a ‘mask’ bit, indicating whether a valid TSF segment existed or not. Collection of these 153 mask bit is recorded as a part of the event data. Also, the 4-bit cell locations and 4 leading bits of phi locations of the 12 ‘seed’ segments, i.e. those in the middle 2 sectors of superlayers 7 and 10, are recorded.

The circular buffer is implemented as a (153+96) bits x 64 words of memory. The event buffers are (153+96) bits x 8 words x 4 buffers. These buffers reside in the Receiver/Decoder FPGA.

2.2 Output DAQ Memory

The output from each ZPD module is 8 bits per CLK4. In addition, we record 28 bits of information for each of the 12 fitted tracks as well as 8 decision bits:

- z_0 (8 bits)
- z_0 error (4 bits)
- curvature (8 bits)
- $\tan I$ (8 bits)
- decision bits (8 bits)

This makes the data size (344+8) bits per CLK4. All data are conveniently available in the Decision Module.

The circular buffer is implemented as a (344+8) bits x 64 words of memory. This fits in two RAM blocks. The event buffers are (344+8) bits x 8 words x 4 buffers.

3 Event Data Format

The total data size from one ZPD module is 601 bytes/event. However,

¹ <http://www.slac.stanford.edu/BFROOT/www/Detector/Trigger/upgrade/docs/zpd/doc/ZpdEventData.pdf>

- The data is to be preceded by a 4-byte event header.
- It is desirable to make the data fit on the 32-bit boundaries. This is to avoid byte swapping in the feature extraction.
- There must be a 32-bit “gap” between the data from the input and output DAQ memories. This is due to 1) the time it takes to switch from one block of memory to the other and 2) the byte swapping in the feature extraction.

Taking these conditions into account, the proposed data format is shown in the table below. The gray boxes represent the padding, and their values are undefined. The total data size including the event header is 680 bytes/event per module.

LSB								→								MSB							
1	1	tag[0:4]							counter[0:4]						bf[1:0]								
CSR[15:0]																							
z0(0,0)[0:7]								error(0,0)[0:3]															
curvature(0,0)[0:7]								tandip(0,0)[0:7]															
z0(0,1)[0:7]								error(0,1)[0:3]															
curvature(0,1)[0:7]								tandip(0,1)[0:7]															
...																							
z0(0,11)[0:7]								error(0,11)[0:3]															
curvature(0,11)[0:7]								tandip(0,11)[0:7]															
decision(0)[0:7]																							
z0(1,0)[0:7]								error(0,1)[0:3]															
curvature(1,0)[0:7]								tandip(1,0)[0:7]															
...																							
z0(7,11)[0:7]								error(7,11)[0:3]															
curvature(7,11)[0:7]								tandip(7,11)[0:7]															
decision(7)[0:7]																							
mask(0)[0:15]																							
mask(0)[16:31]																							
...																							
mask(0)[144:152]																							
cellloc(0,0)[0:3]				phi(0,0)[2:5]				cellloc(0,1)[0:3]				phi(0,1)[2:5]											
...																							
cellloc(0,10)[0,3]				phi(0,10)[2:5]				cellloc(0,11)[0:3]				phi(0,11)[2:5]											
mask(7)[0:15]																							
...																							
cellloc(7,10)[0,3]				phi(7,10)[2:5]				cellloc(7,11)[0:3]				phi(7,11)[2:5]											

The variables in the tables represent:

- tag = trigger tag (5 bits),
- counter = trigger time counter (5 bits),
- bf = buffer number (2 bits) – **MSB first**,
- CSR = CSR (16 bits) – **MSB first**,
- mask(T) = input TSF segment mask (153 bits/tick),
- $z_0(T,F)$ = z_0 (8 bits/track),
- error(T,F) = z_0 error (4 bits/track),
- curvature(T,F) = track curvature (8 bits/track),
- tandip(T,F) = $\tan I$ (8 bits/track),
- decision(T) = output to GLT (8 bits/tick),
- celloc(T,F) = cell location of seed segments (4 bits/track)

where T is the CLK4 tick number (0..7) and F is the track number (0..11) in each tick defined as:

F	SL(seed)	order	sector
0	10	0	2
1	10	0	3
2	10	1	2
3	10	1	3
4	10	2	2
5	10	2	3
6	7	0	2
7	7	0	3
8	7	1	2
9	7	1	3
10	7	2	2
11	7	2	3

3.1 Dependency on daq_format

The DAQ data format from the ZPD can be modified by the daq_format signal (2-bit wide CSR values). This feature is used to implement shorter version of the DAQ data, as well as to help debugging of the ZPD firmware. The current implementations are:

- daq_format = 0 (debug mode)

ZPD returns the test data from the memory address of 0x4000–0x4003, 0x4004–0x4007, 0x4008–0x400B, 0x400C–0x400F in the decision module and from the memory address of 0x4000–0x4002, 0x4004–0x4006, 0x4008–0x400A, 0x400C–0x400E in the decoder driver. Note that these address spaces are normally used as the diagnostic memory. The total size is 20 bytes/event per module.

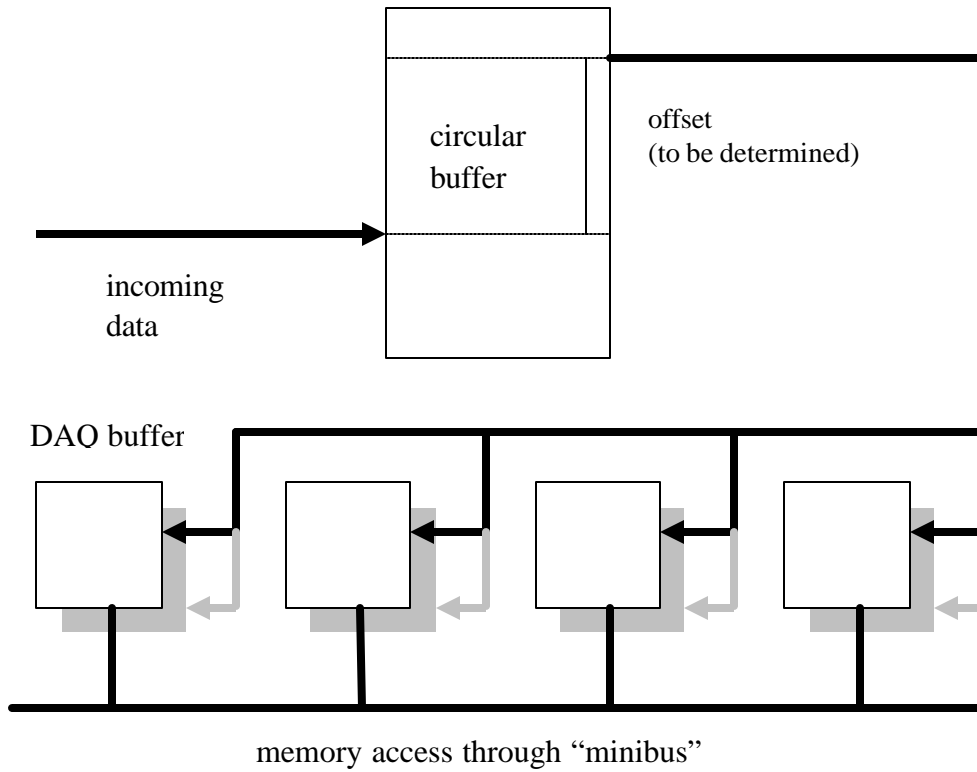
- **daq_format = 1 (Full DAQ data mode)**
ZPD returns the data from the decoder driver and the decision module. This corresponds to the entire data set described in the above table and the total size is again 680 bytes/event per module including the header.
- **daq_format = 2 (short DAQ data mode)**
ZPD returns the data from the decoder driver (*celloc and phi information only*) and the decision module. One may utilize this mode in order to reduce the size of the DAQ data shipped to the readout module. The total size is reduced to 520 bytes/event per module including the header.
- **daq_format = 3 (smallest DAQ data mode, decision module DAQ data only)**
ZPD returns the data from the decision module only. Since it returns the data from the decision module only, there is no padding. The total size is reduced to 420 bytes/event per module including the header.

4 Implementation of the DAQ Memories

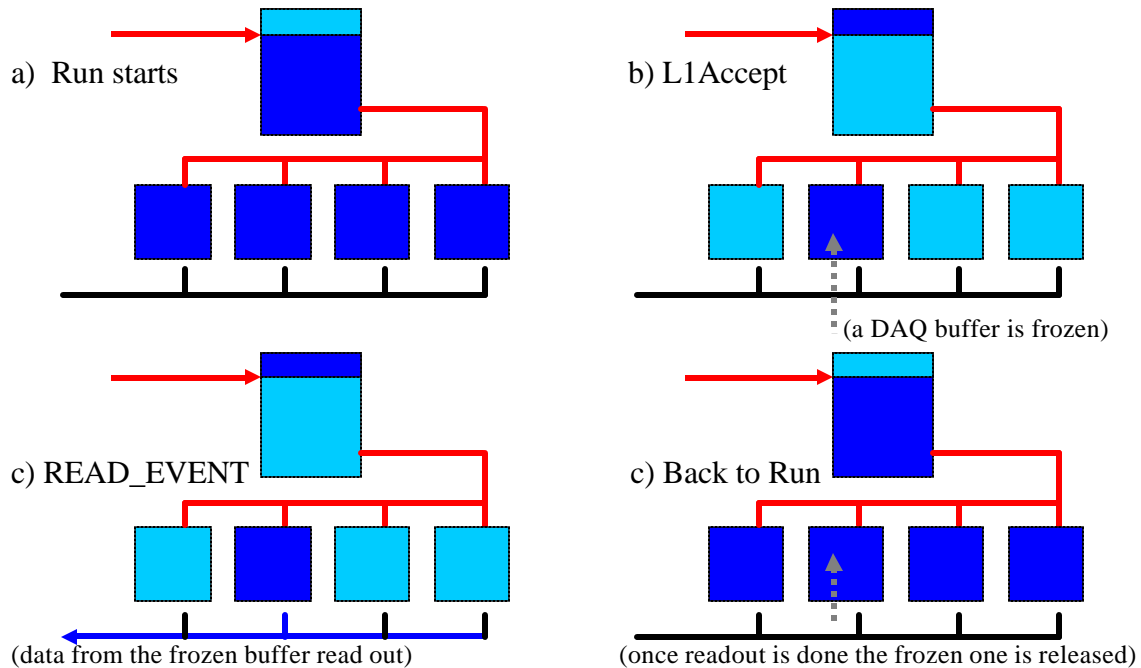
The DAQ memories consist of one 64 event deep circular buffer and of four 8 event deep “DAQ buffers,” as shown in the figure below.

The depth of the circular buffer and the DAQ buffer correspond to 17.2 μ s and 2.2 μ s, respectively. The circular buffer in the decoder driver is 16 bit wide but the one in the decision module is 32 bit wide in order to avoid serialization of the data. Two RAM blocks are used in the implementation of each circular buffer utilizing a double buffering method. The DAQ buffers are all 16 bit wide and one RAM block per buffer is used.

All the memory buffers are implemented utilizing dual port RAM blocks and in total, 15% and 32% of the resource capacities are used in the decoder driver and the decision module, respectively.



The behavior of the DAQ memory can be summarized as follows. Once a run starts, the circular buffer is filled. Data from the circular buffer is *also* copied to the four DAQ buffers with an offset to the pointer of the circular buffer during the run (a) in the figure).



This offset is to be determined during the commissioning phase. In the event that L1Accept is received ((b) in the figure above), one DAQ buffer is frozen and is available to be read out. When a READ_EVENT is received subsequently (c), the DAQ data from the frozen buffer is then read out and is released from the frozen state. Finally, the DAQ memory becomes a normal state as is shown in (d).

The fact that the DAQ buffer is also filled prior to the arrival of L1Accept is a new feature and relevant fast control parts are rewritten in order to meet this new requirement.