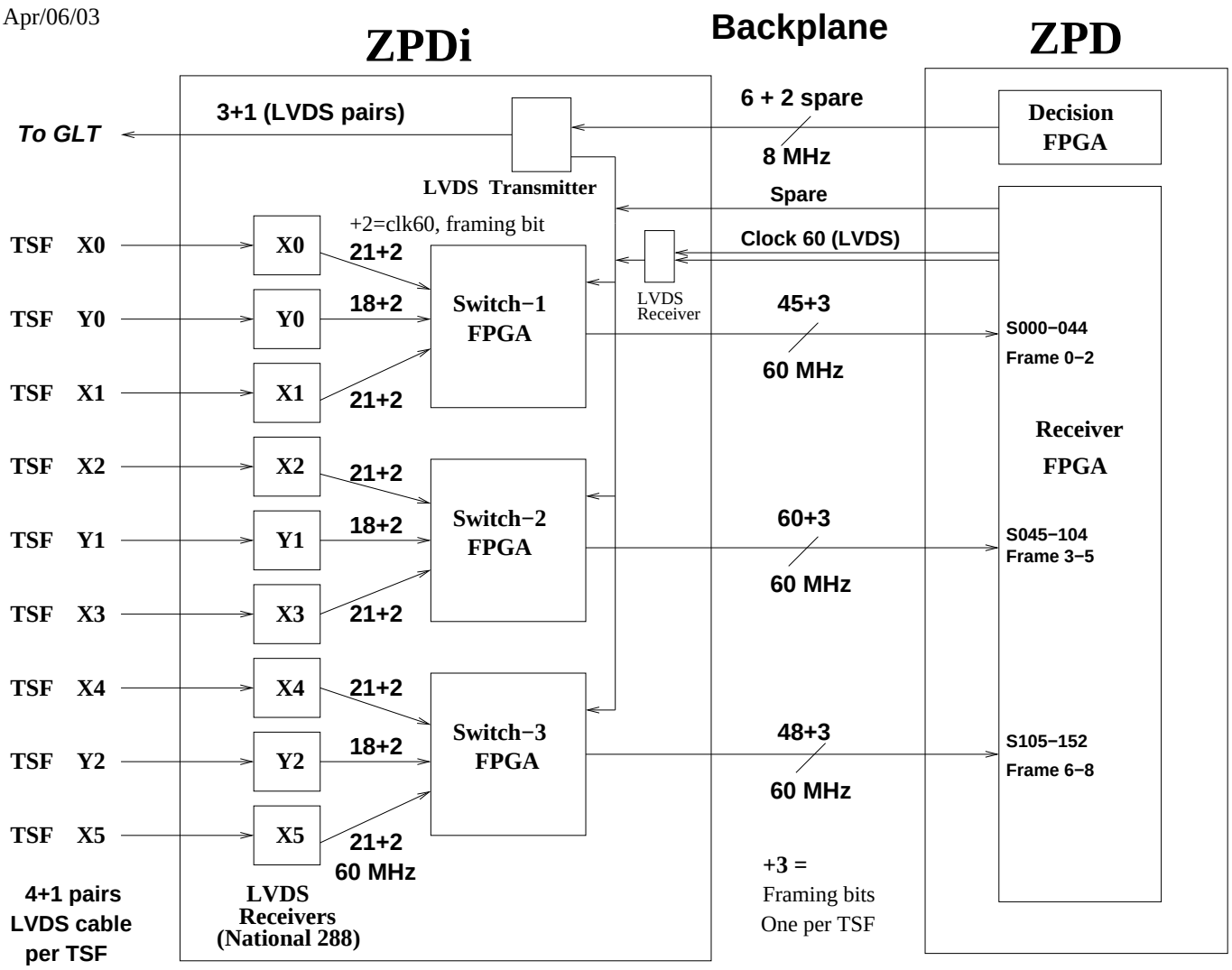
Apr/06/03


ZPDi
Backplane
ZPD
To GLT
3+1 (LVDS pairs)
6 + 2 spare
8 MHz
Decision FPGA
LVDS Transmitter
Spare
+2=clk60, framing bit
Clock 60 (LVDS)
TSF X0
TSF Y0
TSF X1
TSF X2
TSF Y1
TSF X3
TSF X4
TSF Y2
TSF X5
X0
Y0
X1
X2
Y1
X3
X4
Y2
X5
21+2
18+2
21+2
21+2
18+2
21+2
21+2
18+2
21+2
60 MHz
Switch−1 FPGA
Switch−2 FPGA
Switch−3 FPGA
LVDS Receiver
45+3
60 MHz
60+3
60 MHz
48+3
60 MHz
S000−044
Frame 0−2
Receiver FPGA
S045−104
Frame 3−5
S105−152
Frame 6−8
4+1 pairs
LVDS cable
per TSF
LVDS
Receivers
(National 288)
+3 =
Framing bits
One per TSF