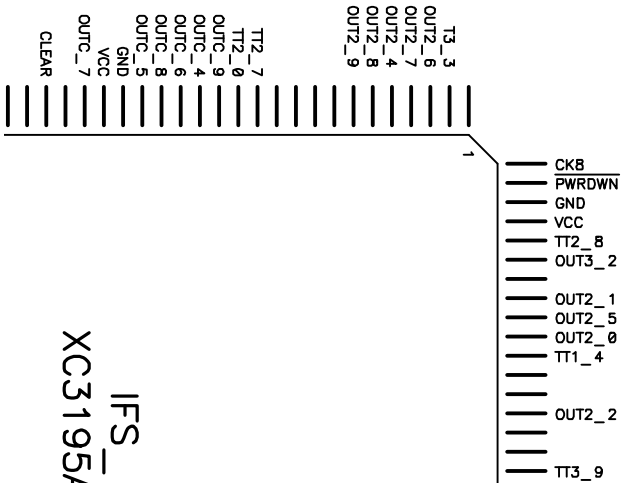
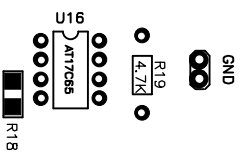
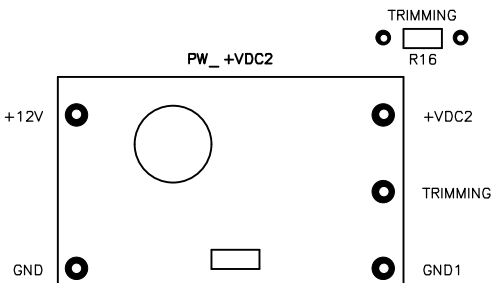
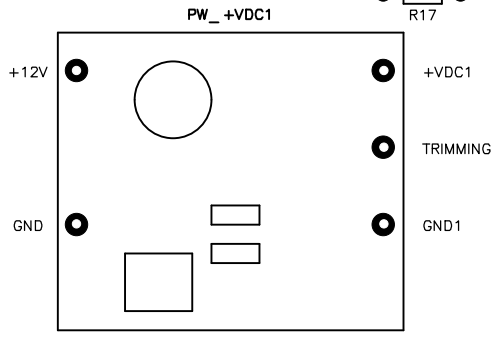
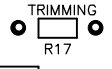
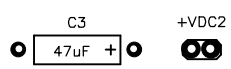
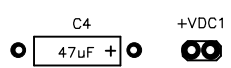
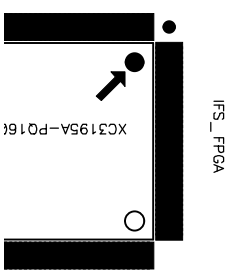


IN HCPL PIN2  OUT HCPL PIN6 

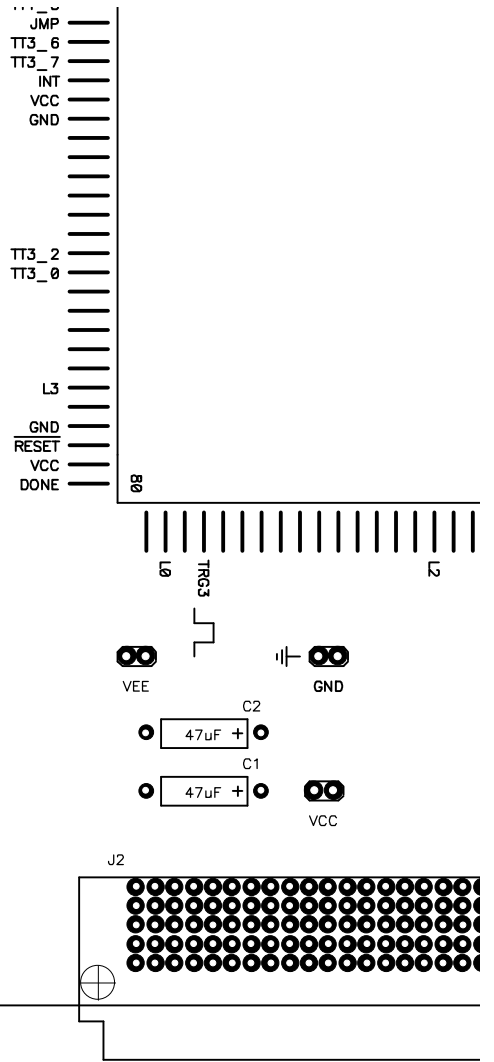


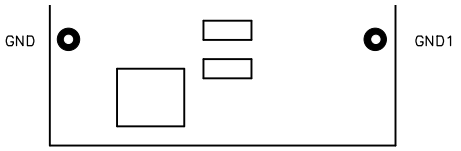
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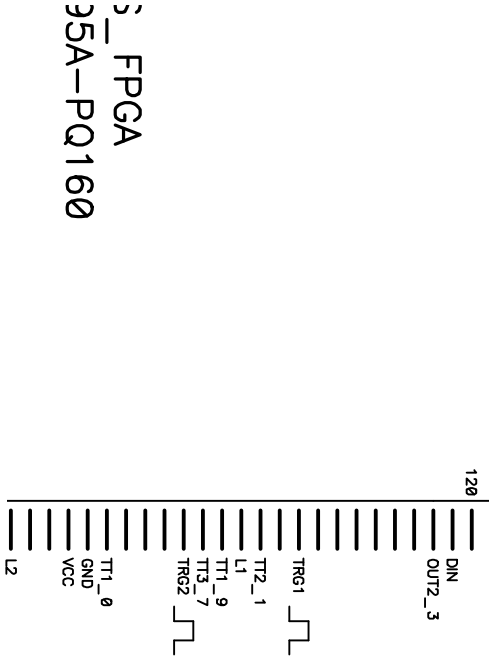
V1.0 13 JUL

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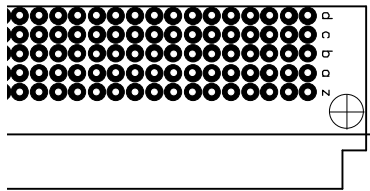




- TT3\_9
- TT2\_3
- VCC
- GND
- TT2\_5
- TT3\_1
- TT1\_1
- TT1\_2
- TT2\_4
- TT1\_3
- TT2\_6
- TT2\_2
- TT1\_8
- TT1\_6
- GND
- VCC
- CCLK



5\_FPGA  
35A-PQ160



SLKTOP MASKTOP

