"Low-level" alarm - direct
"Low-level" alarm - delayed
"Low-level" alarm - latched delayed
"2 out of 4" alarm - direct
"2 out of 4" alarm - delayed
"2 out of 4" alarm - latched delayed
"3 out of 4" alarm - direct
"3 out of 4" alarm - delayed
"3 out of 4" alarm - latched delayed
"4 out of 4" alarm - direct
"4 out of 4" alarm - delayed
"4 out of 4" alarm - latched delayed

All of the following pins are normally LOW:
J1-13: Broken water sensor cable
J1-38: "0 out of 4" in all 12 bar boxes
J1-40: "1 out of 4" trouble
J1-42: "2 out of 4" trouble
J1-44: "3 out of 4" trouble
J1-46: "4 out of 4" trouble
J1-54: VCCs in rack 5 and rack 38 differ by more than 0.25V
J1-56: VCCs in rack 5 and rack 38 differ by more than 0.5V
J1-58: VCC in rack 5 is below 3.5V, i.e. effectively off

Final logic card outputs (all of them are normally LOW):
J1-60: Low-level alarm, direct
J1-62: Low-level alarm, delayed
J1-64: Low-level alarm, latched delayed
J1-66: "2 out of 4" alarm, direct
J1-68: "2 out of 4" alarm, delayed
J1-70: "2 out of 4" alarm, latched delayed
J1-59: "3 out of 4" alarm, direct
J1-61: "3 out of 4" alarm, delayed
J1-63: "3 out of 4" alarm, latched delayed
(J1-46: "4 out of 4" alarm, direct)
J1-67: "4 out of 4" alarm, delayed
J1-69: "4 out of 4" alarm, latched delayed

For the remaining part of bus pin-out, see the schematic diagram for BATMAN-2

ALARM DELAY EXPLANATION (references to "2 out of 4" alarm delay)

Input of the alarm delay circuit is normally low (<0.5V, typically 0.3V or less). When it goes high (>2.7V, typically 3.4V or more), C2 starts charging with RC=4.4s. Thanks to the positive feedback resistor R18, there is a histeresis on the "+" input of the comparator: its output (U2-2) goes from HIGH (typ. >4.95V) to LOW (typ. <0.1V) when C2 charges to 2.09V; transition from LOW back to HIGH will not then occur until the capacitor discharges to 1.49V. This leads to the following timing:

Minimum time before U2-2 goes LOW when U8-10 goes HIGH: approximately 3.3 sec
(C2 charges from 0.2V to 2.1V, V_in = 3.8V)

Minimum time U2-2 stays LOW when U8-10 goes back to normal (LOW) state: approx. 1.7 sec
(C2 discharges from 2.1V to 1.5V, V_in = 0.2V).

Maximum time U2-2 stays LOW when U8-10 goes back to normal (LOW) state: approx. 4.5 sec
(C2 discharges from 3.8V to 1.5V, V_in = 0.2V).

These timings can be scaled by changing RC (say, 2.2 uF -> 1.0 uF; 2.0M -> 1.0M). Use mylar (polyester) capacitors, as they have lower leakage currents.

INHIBIT will _immediately_ override delay's output, but will not immediately discharge capacitor C2. Please allow enough time (at least 5 sec) for C2 to discharge below 1.5V.

NOTE: If U8-10 randomly jumps between HIGH and LOW, U2-2 will go LOW if U8-10 spends at least 53% of all time in the HIGH state; U2-2 will them o back to normal (HIGH) if U8-10 spends not more than 36% of all time in the HIGH state. Time required for such a transition will grow EXPONENTIALLY as time percentage approaches the threshold value. For example, if after sitting in normal state (LOW) for a long time U8-10 starts jumpimg spending 70% of all time in the HIGH state, the time required for U2-2 to go LOW is approx. 6.3 sec; for 60%, it's approx. 9.3 sec. If this is unacceptable, decrease RC.

NOTE: Please do not worry about TLC339's input bias currents. They are typicallly in the picoampere range. DO NOT substitute it with LM339!

NOTE: the "Low-level" ("Warning") alarm will go off if pin 38 on the bus ("0 out of 4 in all 12 bar boxes") goes HIGH. If the mainboard is functioning properly, pin38 = (pin40 OR pin42 OR pin44 OR pin46), i.e. the "Low-level" alarm includes all higher-level alarms. On the other hand, if something is broken, this provides an extra opportunity to detect a malfunction.

To realize this functionality, put a wire jumper between U6-2 (P6) and J1-38 (P7). Otherwise, put a jumper wire between U6-2 (P6) and power ground (P8). DO NOT let U6-2 float!

"4 out of 4" alarm delay
"4 out of 4" alarm latch

Q goes HIGH, and Q-bar goes LOW, when SET is pulled to power ground
Q-bar goes HIGH, and Q goes LOW, when RESET is pulled to power ground
The normal state is the reset state (Q is LOW, Q-bar is HIGH, U14-2 is HIGH, U14-4 is LOW)

U6-6 is normally HIGH
U7-10 is normally LOW
U6-12 is normally HIGH
U8-1 is normally LOW
U2-13 is normally HIGH
U8-4 is normally LOW
U14-6 is normally HIGH

Low-level alarm ("warning")
Warning alarm delay
Warning alarm latch

Q goes HIGH, and Q-bar goes LOW, when SET is pulled to power ground
Q-bar goes HIGH, and Q goes LOW, when RESET is pulled to power ground
The normal state is the reset state (Q is LOW, Q-bar is HIGH, U14-2 is HIGH, U14-4 is LOW)

NOTE: Jo-13 (P1) must be connected with a wire jumper to one of the following places:

J1-54 (P2) or J1-56 (P3) or J1-58 (P4) or 0 Volts (P5) (the latter disables triggering of the low-level alarm in case of problems with power in Rack 5)

"2 out of 4" alarm
"2 out of 4" alarm delay
"2 out of 4" alarm latch

U6-8 is normally HIGH
U8-10 is normally LOW
U2-2 is normally HIGH
U8-13 is normally LOW

Q goes HIGH, and Q-bar goes LOW, when SET is pulled to power ground
Q-bar goes HIGH, and Q goes LOW, when RESET is pulled to power ground
The normal state is the reset state (Q is LOW, Q-bar is HIGH, U14-8 is HIGH, U14-10 is LOW)

"3 out of 4" alarm
"3 out of 4" alarm delay
"3 out of 4" alarm latch

U9-1 is normally HIGH
U9-4 is normally LOW
U2-14 is normally HIGH
U9-10 is normally LOW

The normal state is the reset state (Q is LOW, Q-bar is HIGH. U16-2 is HIGH. U16-4 is

Q goes HIGH, and Q-bar goes LOW, when the switch is thrown to A
Q-bar goes HIGH, and Q goes LOW, when the switch is thrown to B
The normal state of the switch is A (Q is HIGH, U7-2 is LOW, U7-4 is HIGH)
State B (Q-bar HIGH, U7-2 is HIH, U7-4 is LOW) will be used to inhibit "trouble" output of the final logic stages.

Please note that when power is turned on, the flip-flop is forced into the normal (no INHIBIT) state (HIGH Q). This might be useful if the switch is malfunctioning. However, for the first 0.7 sec this is

Q goes HIGH, and Q-bar goes LOW, when the switch is thrown to A (normal state)
Q-bar goes HIGH, and Q goes LOW, when the switch is thrown to B (button pushed)
The normal state of the switch is A (Q is HIGH, U7-6 is LOW, U7-8 is HIGH)
State B ("RESET") (Q-bar HIGH, Q is LOW, U7-8 is LOW) will be used to reset latches

Please note that U12B is used to combine the push-button RESET with the power-on RESET. 12-8 is HIGH if either U4-8 is LOW or U7-8 is LOW. Power of one 7404 inverter should be more than enough to reset all latches.

Switch debouncer for INHIBIT
Switch debouncer for reset

To be on the safe side, use a Texas Instruments part (SN74S140), not National Semiconductor's DM74S140

For roughly 0.7 second after power come up, the output of the comparator stays low, and then goes high. This signal, buffered by SN74S140 drivers, is used to bring all flip-flops to a certain state - just in case...

Power-On reset generator

Since switch S1 is not PC-mountable, we have to connect it to the board with jumper wires

Title	BATMAN-5: The final logic card for the DIRC safety system		
Size: B	Number: Designed by Sasha Telnov (avtelnov@lbl.gov)		Revision: 1.3
Date: 20-Sep-1998		Sheet of	
File: G:\telnov\protel\batman5_4y.Sch		Drawn By:	