

Fast Control Gate Generator

Matt Weaver
SLAC

A new fast control module was added to the master crate to allow programmable sequences of signals to be generated as inputs to the partition masters and gate module. This module is called the fast control gate generator (FCGG).

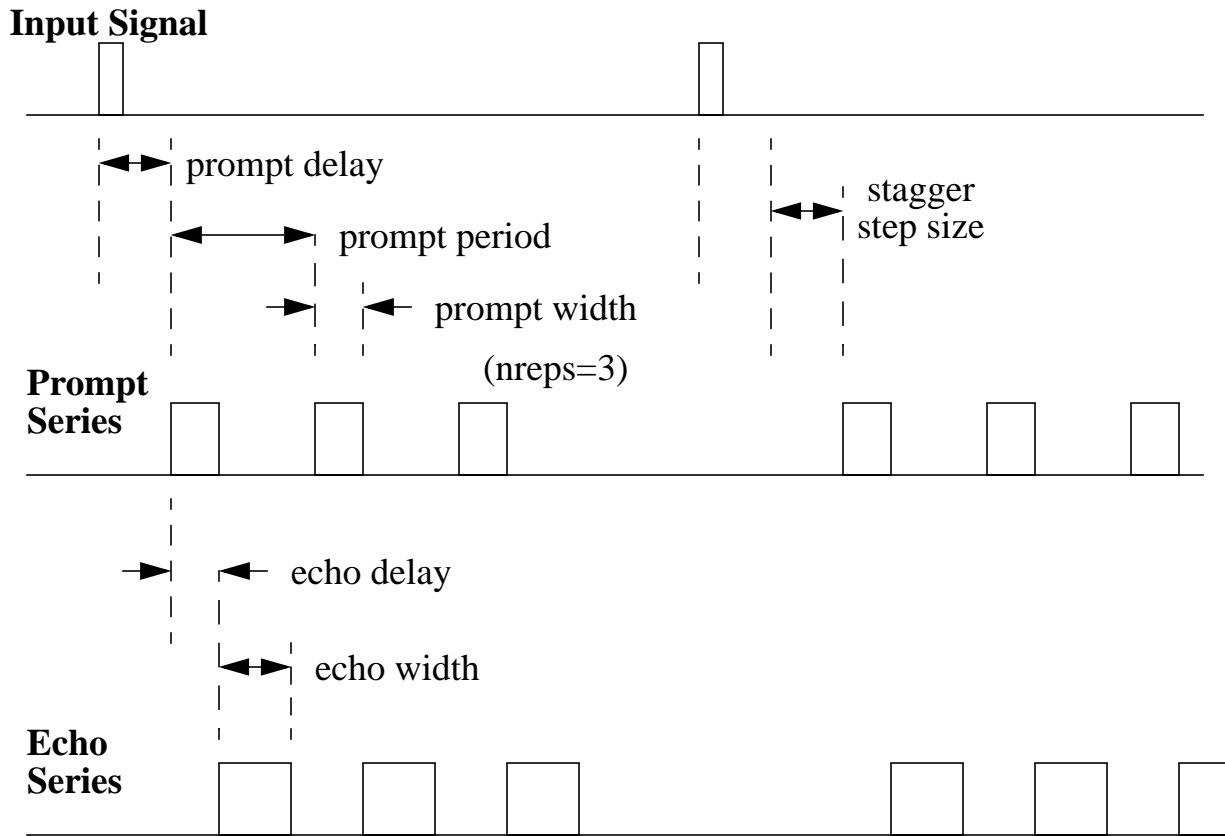
The FCGG has 4 sequencer inputs, 4 sequencer outputs, 2 global inhibit inputs, and 10 partition inhibit outputs. Eight programmable sequencers run in an FPGA which interfaces with these front-panel signals as well as the VME bus and 59.5 MHz system clock on the module backplane. The sequencers are programmed by accessing their registers through 4-byte VME memory operations. The base VME address is determined by a set of dip switches on the module.

The programmable sequencers generate a series of pulses with a fixed timing relationship to the external inputs or a VME write access to the test fire register bit. The sequencer pulses are then logically combined to create the external outputs. Similarly, the external inhibit outputs are a logical combination of the global inhibit inputs and the sequencer pulses. Tables 1 through 4 list the set of registers which control these operations.

Each sequencer has an input control register with 6 active bits. The value of the LSB in the input control register determines whether the sequencer is active; i.e. whether it responds to external inputs or a write to the next LSB - the test fire bit. The next set of 4 bits is a mask of the external inputs which are logically OR'd together to determine the input signal for that sequencer.

$$\begin{aligned} \text{Sequencer 0 Input Signal} = & (\text{External Input 0} \ \& \ \text{mask}[0]) \ | \\ & (\text{External Input 1} \ \& \ \text{mask}[1]) \ | \\ & (\text{External Input 2} \ \& \ \text{mask}[2]) \ | \\ & (\text{External Input 3} \ \& \ \text{mask}[3]) \end{aligned}$$

The series of pulses resulting from a sequencer input signal are described by the sequencer registers in Table 2. Two types of pulses are generated from a sequencer - prompt pulses and echo pulses. Echo pulses are related to prompt pulses by a fixed delay, and they have their own pulse width control as described by the "echo_reg". The series of prompt pulses are generated at a determined delay after the input signal, and they repeat a fixed number of times with a given period and pulse width. The initial delay in this series can be staggered by a fixed step size for a given number of successive input signals after which the initial delay staggering is reset and repeated. Figure 1 shows an example series of pulses with the described parameters.



The sequencer pulse trains can be used to generate the external output signals as well as the inhibit output signals. The output control registers listed in Table 4 are used to OR together the prompt and/or echo pulse trains from any set of sequencers to create the external output signals. The logic driving the external outputs is

$$\begin{aligned} \text{External Output [i]} = & ((\text{Sequencer 0 prompt pulse} \ \& \ \text{out[i_mask[0]}) \ | \\ & (\text{Sequencer 0 echo pulse} \ \& \ \text{out[i_mask[8]}) \ | \\ & (\text{Sequencer 1 prompt pulse} \ \& \ \text{out[i_mask[1]}) \ | \\ & (\text{Sequencer 1 echo pulse} \ \& \ \text{out[i_mask[9]}) \ | \\ & \dots \\ & (\text{Sequencer 7 prompt pulse} \ \& \ \text{out[i_mask[7]}) \ | \\ & (\text{Sequencer 7 echo pulse} \ \& \ \text{out[i_mask[15]})) \end{aligned}$$

The inhibit output signals are controlled by the registers listed in Table 5. The logic driving the inhibit outputs is

$$\begin{aligned} \text{Inhibit Output [i]} = & \text{Inhibit Input 0} \ | \ \text{Inhibit Input 1} \ | \quad \{ \text{global overrides} \} \\ & (((\text{Sequencer 0 prompt pulse} \ \& \ \text{inhibit_mask_in[0]}) \ | \quad \{ \text{included pulses} \} \end{aligned}$$

(Sequencer 0 echo pulse & inhibit_mask_in[8]) |
 (Sequencer 1 prompt pulse & inhibit_mask_in[1]) |
 (Sequencer 1 echo pulse & inhibit_mask_in[9]) |
 ...
 (Sequencer 7 prompt pulse & inhibit_mask_in[7]) |
 (Sequencer 7 echo pulse & inhibit_mask_in[15])) &
 ~ ((Sequencer 0 prompt pulse & inhibit_mask_in[16]) | { excluded pulses }
 (Sequencer 0 echo pulse & inhibit_mask_in[24]) |
 (Sequencer 1 prompt pulse & inhibit_mask_in[17]) |
 (Sequencer 1 echo pulse & inhibit_mask_in[25]) |
 ...
 (Sequencer 7 prompt pulse & inhibit_mask_in[23]) |
 (Sequencer 7 echo pulse & inhibit_mask_in[31])) &
 inhibit_mask_out[i])

Table 1: FCGG Register Sets

Register Set	Base Offset
Sequencer 0	0x00
Sequencer 1	0x10
Sequencer 2	0x20
Sequencer 3	0x30
Sequencer 4	0x40
Sequencer 5	0x50
Sequencer 6	0x60
Sequencer 7	0x70
Input Control	0x80
Output Control	0xA0
Inhibit Masks	0xB0

Table 2: Sequencer Registers

32-bit Register	Offset	Bits	R/W	Description
period_width	0x00	0-19	rw	Period between prompt pulses in sysclk counts

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32-bit Register	Offset	Bits	R/W	Description
period_width	0x00	20-29	rw	Width of prompt pulses in sysclk counts
period_width	0x00	30-31	rw	??
delay_reps	0x04	0-19	rw	Delay before first prompt pulse in sysclk counts
delay_reps	0x04	20-31	rw	Number of prompt pulses
stagger_reg	0x08	0-15	rw	Step size in first pulse delay
stagger_reg	0x08	16-27	rw	Number of steps
echo_reg	0x0C	0- 9	rw	Delay from prompt pulse to echo pulse in sysclk counts
echo_reg	0x0C	10-19	rw	Width of echo pulse in sysclk counts

Table 3: Input Control Registers

32-bit Register	Offset	Bits	R/W	Description
seq0_input_ctl	0x00	0	rw	0/1=Disable/Enable sequencer
seq0_input_ctl	0x00	1	w	1=Single fire of sequencer
seq0_input_ctl	0x00	2-5	rw	Mask of external inputs OR'd together to make sequencer input.
seq1_input_ctl	0x04			
seq2_input_ctl	0x08			
..	..			
seq7_input_ctl	0x1C			

Table 4: Output Control Registers

32-bit Register	Offset	Bits	R/W	Description
out0_mask	0x00	0- 7	rw	Mask of sequencer prompt pulses for external output 0

Table 4: Output Control Registers

32-bit Register	Offset	Bits	R/W	Description
out0_mask	0x00	8-15	rw	Mask of sequencer echo pulses for external output 0
out1_mask	0x04			
..	..			
out3_mask	0x0C			

Table 5: Inhibit Mask Register

32-bit Register	Offset	Bits	R/W	Description
inhibit_mask_in	0x00	0- 7	R/W	Sequencer prompt pulses included
inhibit_mask_in	0x00	8-15	R/W	Sequencer echo pulses included
inhibit_mask_in	0x00	16-23	R/W	Sequencer prompt pulses excluded
inhibit_mask_in	0x00	24-31	R/W	Sequencer echo pulses excluded
inhibit_mask_out	0x04	0- 9	R/W	Mask of inhibit outputs driven