

BaBar DAQ ROM

Untriggered Personality Card Description

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File Name:	JohnD HD:BaBar:Write-Ups:Untriggered Personality Card:Untriggered Personality Card		
First Modified:	7-Mar-97	Last Modified:	23-Jun-97

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2. INTRODUCTION

This document describes the functionality of the untriggered personality module.

This module is used by the calorimeter to receive 'FLINK' data from the front-end ADCs. The data on the FLINKs consists of a steady stream of packets of data, each of which contains the result of the digitisation of twenty-four crystals. The digitisation at the front-ends happens at 3.7MHz (SYSCLK/16), so one packet is sent every 270ns. The untriggered PC first cracks the packet format, then corrects the raw ADC/range data, and sends the sum of energy in each FLINK as a single trigger tower to the level one calorimeter trigger.

Corrected data, trigger tower sum, information about neighbouring PCs and status from the front-end is written into the untriggered version of the Intermediate Store (IS), before being read out in the same way as the triggered PC.

3. EMC-SPECIFIC FUNCTIONALITY

There are up to three FLINKs on an untriggered PC. In the barrel all three are used and connect to the transmitters on the one Barrel I/O Board (BIOB). In the end-cap, because of the greater occupancy of the crystals, only two FLINKs connect to the two transmitters on one End-cap I/O Board (EIOB). Therefore in all cases there is a one-to-one mapping from I/O Board to PC. The electronics associated with the unused FLINK may or may not be loaded on the PC.

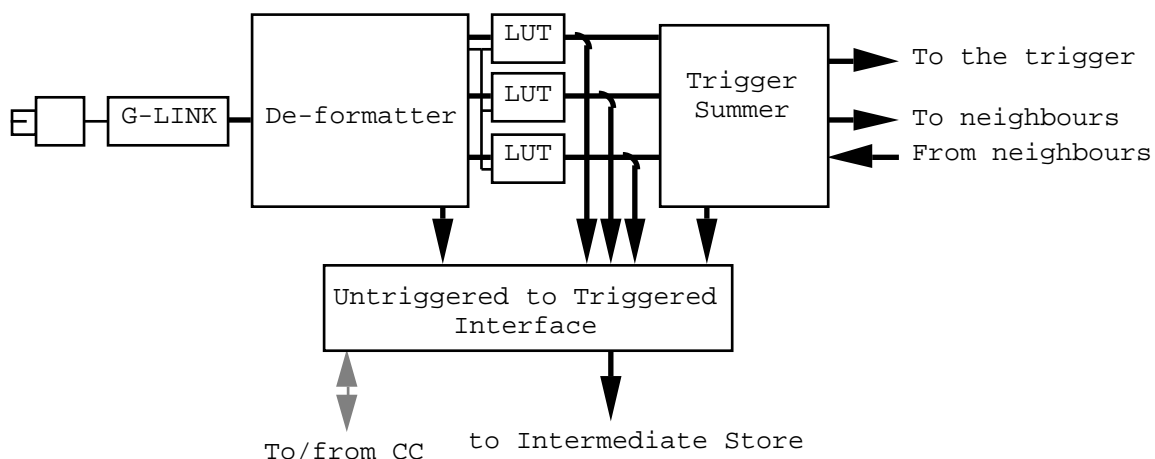


Figure 1 — EMC Specific Functionality

Figure 1 shows a diagram of the EMC specific processing for one FLINK. This is discussed in the next sections.

3.1 Packet Deformatting

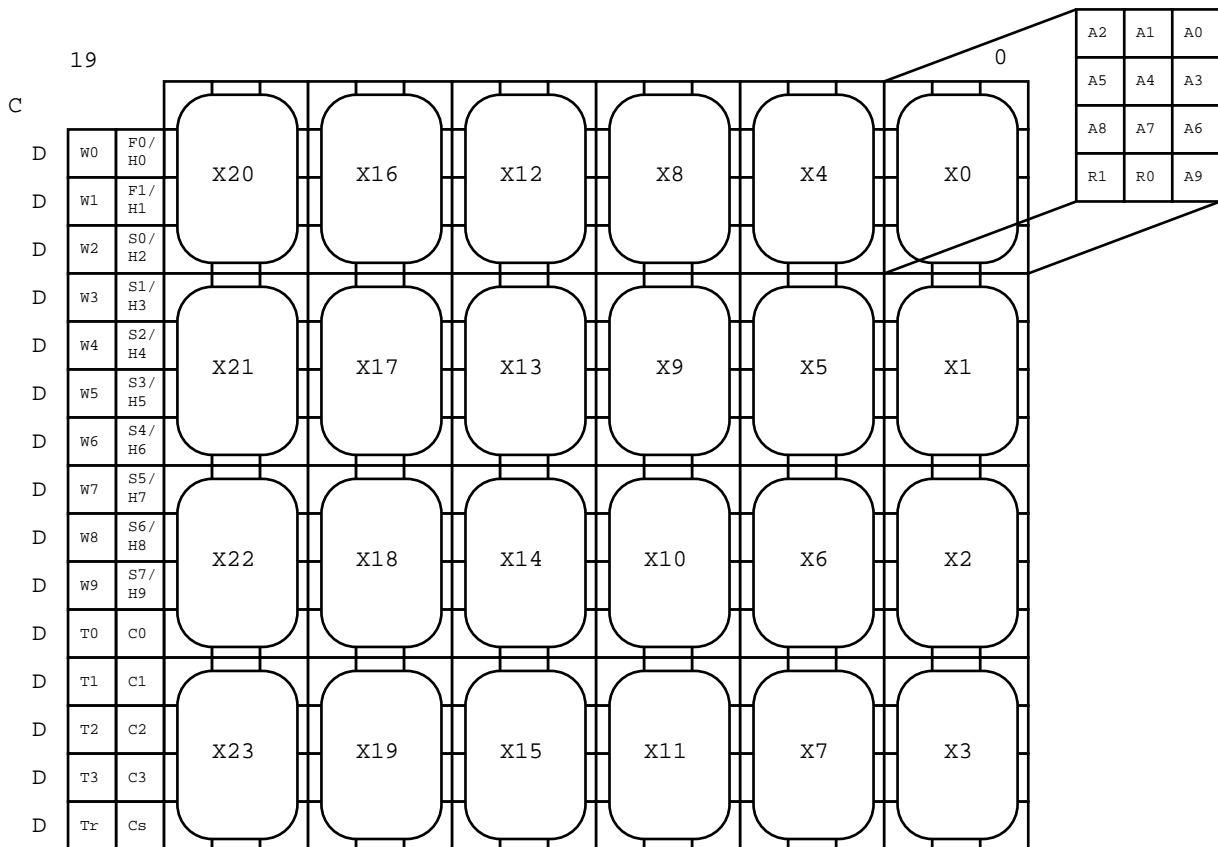


Figure 2 — FLINK Packet Format

The format of a packet received from the FLINK is shown in Figure 2. It is a series of sixteen, twenty bit words (time runs from top to bottom of the figure); the first word is a control word and the rest are data words. The use of a control word as the first word allows automatic synchronisation after link start-up.

The packet contains the following information:

Bits	Description
W9 . . W0	Wall clock, incremented for each packet
F1 . . F0	Fibre number (0, 1, 2).
S7 . . S0	IOB Serial Number.
H9 . . H0	The header of the last message received on the CLINK.
Tr	'1' if a L1Accept was received during the sample period covered by this packet.
T3 . . T0	The phase of the last L1Accept w.r.t. the sample clock.
Cs	'1' if a Cal strobe was received during the sample period covered by this packet.
C3 . . C0	The phase of the last Cal strobe w.r.t. the sample clock.

Note that either F1..F0, S7..S0 or H9..H0 can be sent, but not both at the same time. H9..H0 will be sent during normal running.

These pieces of information are not interpreted by the hardware of the PC, but are made available in the intermediate store. The CPU could use them as follows:

- The wall clock can be used to check the integrity of the packet and perhaps the coarse relative timing of the FLINKs in the system.
- The fibre number and serial number are meant as test features and for checking that the system is cabled correctly. They would not be used during normal data taking.
- The header of the last message received on the CLINK at the IOB is used to get from the front-end the tag that was sent down with the L1Accept. Since the L1Accept is a message on the CLINK it follows that it will be reported in these bits. This tag will be compared with that from the controller card to check for errors.
- The phase of the L1Accept will be compared across the whole system to make sure no IOB gets out of step with the others (since if it does the phase of the L1Accept will wander).

The other bits could be checked or simply reported with the data for later use.

Note that as another test feature it is also possible to instruct the front-ends to send back a test pattern in place of ADC data.

3.2 Data Correction

The digitised data on the FLINK consists of:

- two bits indicating which gain range was digitised:

R1	R0	Gain range
0	0	x1
0	1	x4
1	0	x32
1	1	x256

- The ten bit ADC reading.

Before the digitisation can be used in any calculations it must be converted to a “linear” scale. This is performed by putting the twelve bit digitisation through a Look-Up-Table (LUT) to produce a sixteen bit result. The LUT will be loaded with data from piece-wise linear fits to convert the four gain ranges into an absolute energy scale. The least significant bit of the sixteen bit result may correspond to an energy of 250keV.

Because the pre-amp output is AC coupled the digitised pulse shape will go negative for some part of its duration. This undershoot is important for the digital filter, so the LUT must be able to accommodate “negative energy”. This could be done by defining its output as a sixteen bit signed integer, however this reduces the dynamic range to fifteen bits. In order to preserve the maximum dynamic range the output of the LUT is defined as “offset-binary”, i.e. the true energy plus an offset.

The LUT will also produce two ‘flags’ (described later):

- ADD This bit will be used in the generation of the trigger tower energy sum.
- FEX This bit will be used in the determination of the selective feature extraction flag.

It is currently anticipated that these two bits will be defined to mean ‘corrected energy above a given threshold’, with the FEX threshold lower than the ADD threshold.

3.3 Trigger Tower Generation

The crystals served by one FLINK correspond the crystals in one trigger tower. The trigger tower energy sum is calculated for each sample period from the corrected energies as follows:

```
trigger_tower_sum = 0;
try {
    for (crystal_number = 0; crystal_number<24; crystal_number++) {
        if (crystal[crystal_number].add) {
            trigger_tower_sum += crystal[crystal_number].energy - LUT_offset;
        }
    }
}
catch (IntegerOverflowException e) {
    trigger_tower_sum = 0xFFFF;
}
```

As you can see the ADD bit from the LUT is used to gate the crystal into the sum and the offset in the energy scale in the LUT must be subtracted before adding into the sum. The ADD bit can be used to exclude crystals from the sum either if they are noisy or dead or don't exist. Not all FLINKs in the end-cap cover twenty-four crystals, some cover only twenty-two or twenty-three.

If an overflow occurs in the accumulation then the trigger sum must saturate at full scale.

3.4 Generation/Distribution of Occupancy Information to Neighbouring PCs

Note this is not yet final.

Before feature extracting each crystal, software in the CPU will check whether the FEX bit of the crystal or the FEX bit of any of its eight neighbours has been '1' in a given window around the nominal trigger time. If not, the crystal will not be feature extracted. This lowers the load on the CPU.

If a crystal is on the edge of the area covered by an FLINK then the FEX bits for some of its neighbours will need to be communicated from the neighbouring FLINK. To minimise the amount of interconnection the FEX bits along the edges are first ORed before being sent to the neighbouring FLINK, as shown below, to give ten edge FEX bits: north1, north2, north-east, east, south-east, south1, south2, south-west, west and north-west.

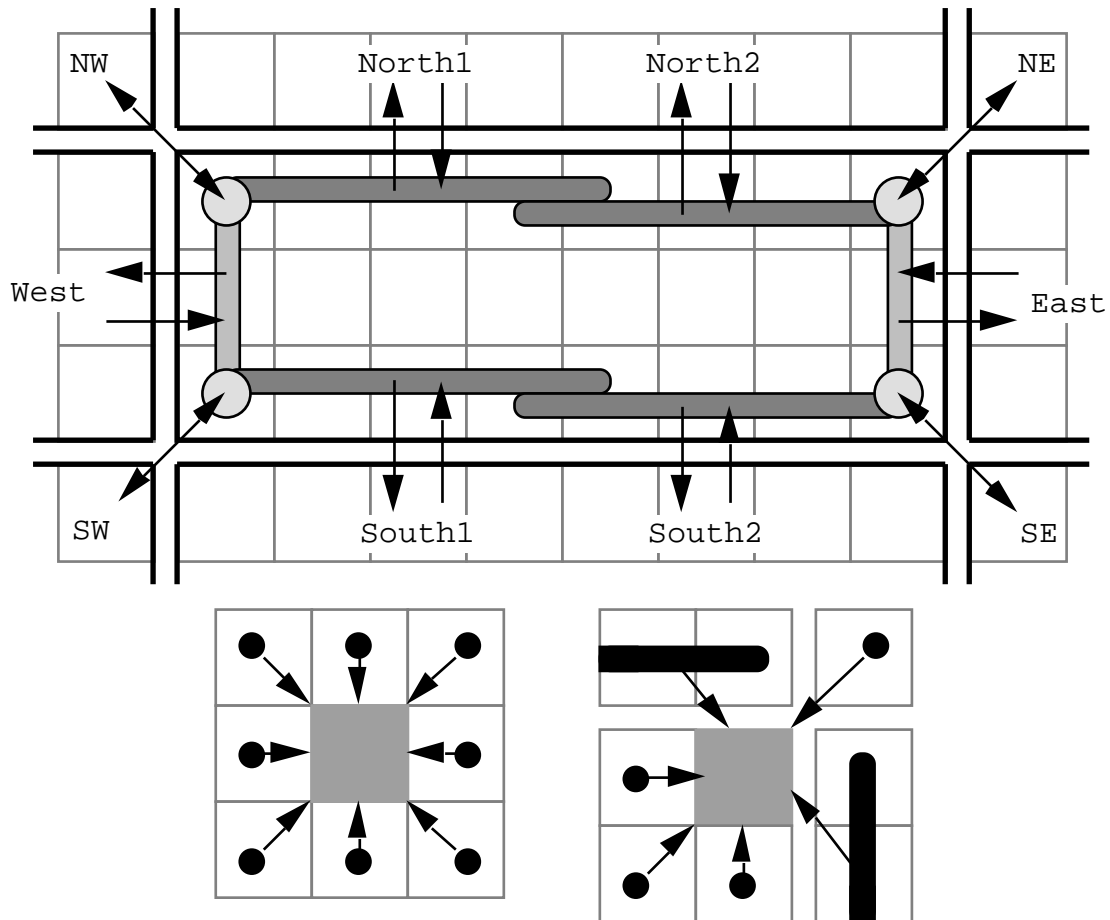


Figure 3 — Neighbour Interconnect (barrel shown)

As shown in the diagram in the bottom left of Figure 3, if all neighbours of a crystal are in the same FLINK then the FEX bits for all eight neighbours are directly available. The example in the bottom right of Figure 3 shows a crystal in the corner of the area covered by an FLINK. In this case the neighbours in other FLINKs are approximated by the edge FEX bits shown.

The sharing of these flags must be performed between FLINKs on the same PC, FLINKs on PCs in the same crate and FLINKs on PCs in different crates. All ten edge FEX bits for each FLINK are connected to the J3 backplane via the CC and, likewise, so are the ones in the reverse direction. This allows the logic on the PC to be independent of where the crystals it serves are in relation to the rest of the system: it is all sorted out on the backplane.

4. INTERFACE TO THE ROM

Because of the high bandwidth required on the i960/PCI busses to get the contents of the intermediate store into CPU memory, the following mechanism is provided by the PC for use by the DMA unit in deciding whether to DMA the data for a given L1Accept or not (this data is available for each FLINK individually). Two flags are computed in hardware:

- LOCAL_FEX is '1' if any of the FEX bits for the crystals in the FLINK is '1' in any of the samples stored for this L1Accept.
- NEIGHBOUR_FEX is the same as LOCAL_FEX, but for the incoming neighbour FEX bits.

These flags need not be used if you don't need them or trust them, but if they are used:

- During source calibrations only LOCAL_FEX should be used to decide whether to DMA the data or not.
- During normal running the the logical OR of both FEX bits should be used.

4.1 Interface to the Controller Card

The untriggered PC does not look very different from the triggered PC from the point of view of the CC, with the following exceptions:

- Front-end register reads do not exist. If RX_READ is asserted by the CC the PC will assert DONE and PC_END, indicating that the read has finished and there is no data to transfer from the IS. Issuing a front-end register read to the untriggered PC is, however, an error!
- The CC has eight link status inputs, labelled for two C/D-LINK pairs. The untriggered PC has three FLINKs and no CLINKs. The link status signals are connected as follows. The status signals from each FLINK can be gated inactive by bits in a control register. Note that the CLINK ready inputs are tied active (logic '0') and the status signals for FLINK C are placed on the CLINK locked inputs.

CC input	Status signal
nCLRDYA	'0'
nCLRDYB	'0'
nDLRDYA	FLRDYA
nDLRDYB	FLRDYB
DLERRA	FLERRA
DLERRB	FLERRB
nCLLCKA	FLRDYC
nCLLCKB	FLERRC

The untriggered PC responds only to the following CLINK commands:

CLINK command	Opcode	Action
Sync	2	Used in the interface to the trigger, discussed later.
Spy Start	6	Initiate test sequence to trigger, discussed later.

Clear Readout is not used to clear the intermediate store because even though there will be no L1Accepts still being written into the IS when it is asserted, there could still be L1Accepts in the IS

waiting to be read out over the i960. For this reason clearing the untriggered IS is performed at a higher level using software writing to a reset register on the PC (see later).

When the CC issues the `RX_DATA` to the untriggered PC, the PC responds with `DONE` and a status. The bits in the status word are defined as follows:

Bit	Definition
7:3	Undefined, set to '0'.
2	'1' if timeout before FLINK C data is in IS, '0' otherwise.
1	'1' if timeout before FLINK B data is in IS, '0' otherwise.
0	'1' if timeout before FLINK A data is in IS, '0' otherwise.

The words in the transfer result are defined as follows (all words are always present even if one times out, in which case the result is 0):

Word	Definition
0	FLINK A result.
1	FLINK B result.
2	FLINK C result.

Where the bits in the transfer result for each FLINK are defined as shown below:

Bit	Definition
15	'1' if any of the FEX bits in this FLINK were asserted in the data corresponding to this L1Accept.
14	'1' if any of the FEX bits in this FLINK's neighbours were asserted in the data corresponding to this L1Accept.
13	'1' if any of the LRDY/ERROR bits were asserted in the data corresponding to this L1Accept.
12:0	Offset in the intermediate store of the start of data for this L1Accept.

4.2 The Untriggered Intermediate Store

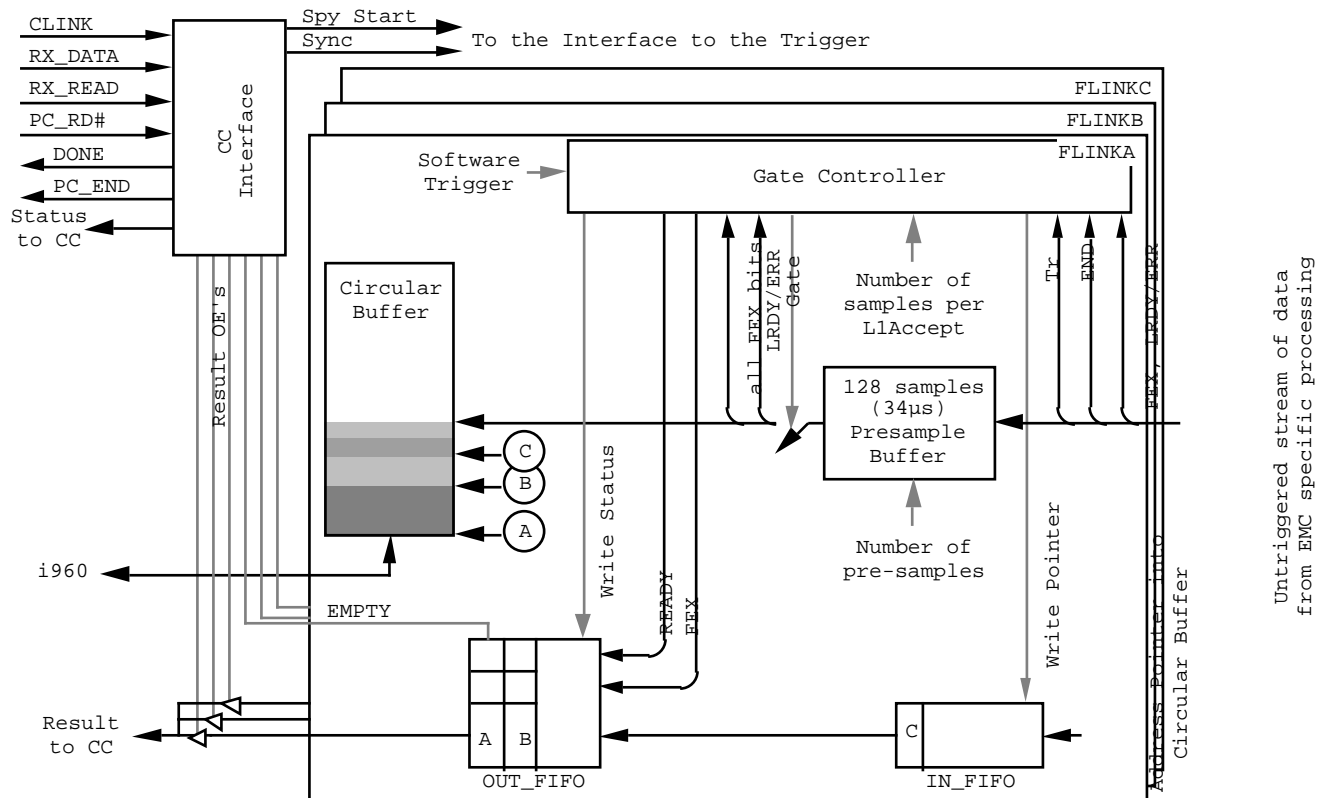


Figure 5 — Interface to the Intermediate Store

Figure 5 shows the interface to the Intermediate Store (and hence the i960) from the EMC specific section of the PC. As shown, most processing is performed for each FLINK independently, only being combined at the interface to the CC.

To write the desired samples into the circular buffer when an L1Accept occurs the following happens:

- The untriggered stream of samples from the EMC specific processing is delayed in a pre-sample buffer whose depth is programmable (in number of samples) via a register.
- A ‘gate controller’ spys on the Tr bit in the packets going into the pre-sample buffer (see the packet format in Figure 4). When Tr is asserted it means that a L1Accept was received at the front-end over the CLINK during that sample period. This will happen a fixed time after the interaction that produced the L1Accept.
- After the gate controller sees the Tr bit is high it ‘closes’ the gate into the circular buffer for a specified number of samples (the number of samples per L1Accept, set in a register). This writes the data into the circular buffer. By adjusting the depth of the pre-sample buffer the number of samples before and after the peak can be adjusted.
- When the gate is closed the gate controller writes the offset at which writing starts into the “IN_FIFO”. In the figure you can see the offset corresponding to L1Accept ‘C’ in this FIFO. The number of addresses in the IN_FIFO corresponds to the number of overlapping L1Accepts that are currently being processed.

- While the samples are being written into the circular buffer the 'Linkready/Error' bit is accumulated by the gate controller into the signal 'READY' in the figure. In other words, if this bit is '1' in any of the words in any of the samples then READY is '1'. Similarly the FEX bits for all crystals and those that have come from neighbouring FLINKs are accumulated into the 'FEX' bit.
- When all samples for the L1Accept have been written into the circular buffer the gate controller writes the offset from the IN_FIFO and the two accumulated status bits into the OUT_FIFO.

It is also possible to 'trigger' the gate controller from software (this feature can be disabled by a bit in a register) as if it had seen the T_r bit. This may be used for source calibration, but certainly as a test mode.

Therefore, unlike the triggered PC, an L1Accept moves the data into the Intermediate Store and stores the result (start offset, READY, FEX) in the OUT_FIFO. When the CC subsequently asserts RX_DATA all that is required is for the result to be transferred. So the sequence of events is as follows:

- When RX_DATA is asserted, the CC Interface waits until the OUT_FIFOs of all enabled FLINKs are not empty. Then it asserts DONE. Since the contents of the packets are decoded to find L1Accepts there are numerous things that could go wrong with the result that at least one gate controller does not recognise the L1Accept. For this reason the CC Interface will time-out if all data is not available within a specified time limit, so the status returned to the CC is which (if any) of the enabled FLINKs timed out.

The length of the timeout is approximately $10\mu\text{s}$ plus the length of the data for an L1Accept. For example for 64 samples per L1Accept the timeout is $10 + 64 * 0.27 = 27\mu\text{s}$. This is computed automatically.

- The CC then asserts PC_RD#, to which the CC Interface enables the offset and flags from the OUT_FIFO of FLINK A onto the result bus. This happens twice more (for FLINKs B and C) with the CC Interface asserting PC_END with the result for FLINK C.

To use the buffer model on the CC to regulate this process the following must be observed:

- The maximum number of L1Accepts that can be overlapping will be set by how many accumulators are implemented in the Gate Controller and the depth of the IN_FIFO. This is presently expected to be four. Therefore the maximum number of buffers in the MUQ on the CC is four.
- The maximum number of L1Accepts that can be stored in the IS will be at least the length of the circular buffer divided by the length of data for an L1Accept. The length of the circular buffer will be 4k or 8k sixty-four bit words (depending on which variant of the memory chip is loaded); for the prototype we will use the 8k version. The length of data for an L1Accept during normal data-taking is 512 sixty-four bit words, so the capacity of the IS is sixteen L1Accepts.

In order not to overflow the IS the sum of the number of buffers in the MUQ and TUQ must therefore be sixteen, so the number of buffers in the TUQ is twelve. If the length of data for an L1Accept is extended then the number of buffers in the MUQ and TUQ should be changed accordingly.

Notes:

- The data per FLINK corresponding to one L1Accept is a sequence of between 64 and 512 samples (of the format shown in Figure 4). The number of samples per L1Accept is specified in a register on the PC. Sixty-four samples is the normal mode for data taking, 512 would be used during source calibration.

- Since the amount of data kept for one L1Accept covers a time period from $17\mu\text{s}$ to $136\mu\text{s}$, it is possible for L1Accepts to come close enough that some samples are associated with more than one L1Accept. This is accommodated in the following way: if the Tr bit is high again before all samples are written into the circular buffer the gate controller simply extends the gate to accommodate the new L1Accept. In effect it is a retriggerable monostable.

Just such a case is illustrated in Figure 5. The shading in the circular buffer is meant to indicate the data associated with an L1Accept. Three L1Accepts are outstanding (A, B,C), the address of the start of data has been marked with the corresponding letter. L1Accept 'A' occurred first and all data corresponding to it was written into the circular buffer (shown in grey) with no overlapping L1Accept. However, part way through writing in the data corresponding to L1Accept 'B', L1Accept 'C' occurred.

- Since it is a circular buffer, it is possible for the samples for one L1Accept to wrap around from the end to the beginning of the buffer. So that the DU does not need to do anything special if this happens, the circular buffer is mapped twice into the i960 address space, in two contiguous regions as shown below. This means that although the i960 address may not wrap around, the correct data is transferred.

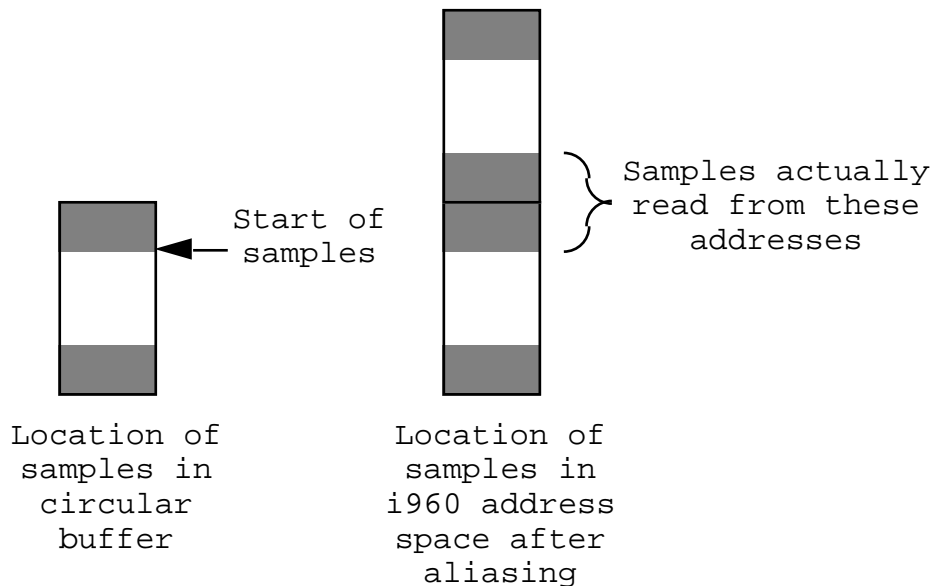


Figure 6 — Aliasing of the Intermediate Store

5. INTERFACE TO THE TRIGGER

Each FLINK computes its own energy sum for each sample period using the clock recovered from the GLINK, the phase of which may differ by tens of nanoseconds from FLINK to FLINK. The interface to the trigger must run from a common clock (in fact the SYSCLK from the CC), so the data must first be re-synchronised to that clock and each other and then sent to the trigger as:

- Bit serial data for each FLINK (sixteen bits at 59.5Mbit/s)
- A common 59.5MHz clock (the SYSCLK)
- A common FRAME bit that indicates the start of each word.

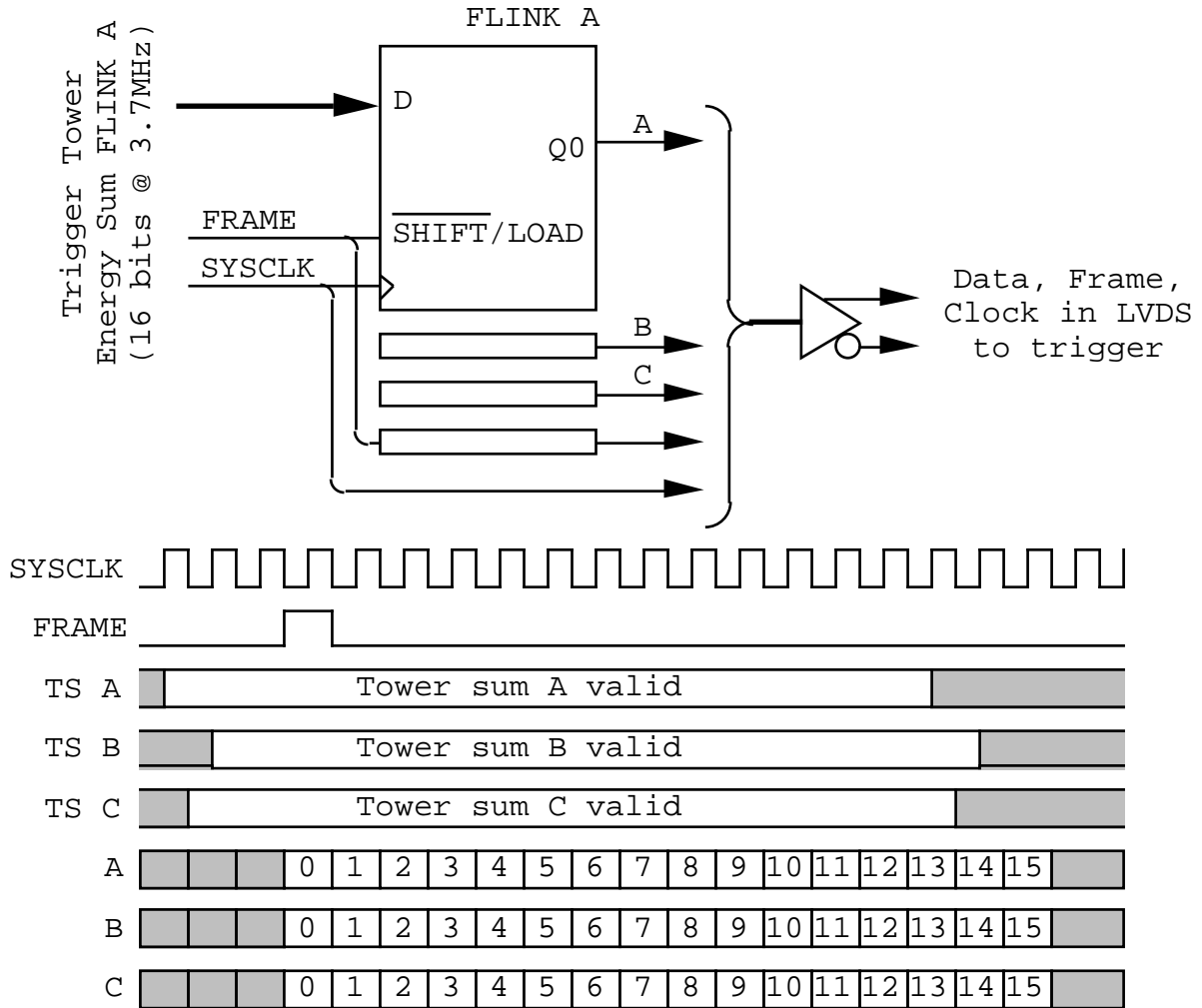


Figure 7 — Interface to the Trigger

Figure 7 shows the interface to the trigger from three independent FLINKs to the common signals on the cable. Since the tower energy sums only change at 3.7MHz the synchronising is done by loading all three outgoing shift registers at the same time (all clocked by SYSCLK) and doing it well away from the transitions in the tower sums.

To generate the FRAME bit a sixteen bit counter is clocked by the SYSCLK and reset by the receipt of a SYNC. FRAME is asserted each time this counter matches a programmable value. The phase of FRAME with respect to the trigger tower sum data can therefore be placed in the correct position.

For testing it is possible to send a test pattern to the trigger instead of the energy sum. When this mode is selected (by a bit in a control register) the reception of the “start playback” command on the CLINK initiates the sending of this sequence once only. If the test mode is selected and the “start playback” command is not active the trigger sum outputs default to all zero.

The sequence sent to the trigger from each FLINK is as follows:

Sequence Number	FA	FB	FC	Frame
0	0	0	1	1
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
...
15	0	0	1	0
16	SERNO[0]	SERNO[0]	SERNO[0]	1
17	SERNO[1]	SERNO[1]	SERNO[1]	0
...
23	SERNO[7]	SERNO[7]	SERNO[7]	0
24	0	1	0	0
25	0	0	1	0
...
31	0	0	0	0

The first word tests cable integrity.

The second word contains the serial number of the module (SERNO[7:0]), and the following two bits specify which FLINK this bit is connected to (0 for A, 1 for B, 2 for C).

6. PC REGISTER MAP

Note that for the moment the register map and bit assignments are for illustration only.

The following table shows the register map. Registers are located at an offset from a base address, the eight most significant (31:24) of which are set by a DIP switch on the PC. The module will only respond correctly to bus accesses that assume a thirty-two bit wide bus, although the byte enables will be used to provide byte-wide addressing.

Offset from Base Address (hex)	Name	Description
0	SERNO	Board location and serial number register
4	CTRL	Module control register.
8	LINK_STAT	FLINK status register
C	TRIGCTRL	Trigger control register.
10	SWTRIG	Triggers the gate controller (if enabled).
200000–3FFFFFF	LUT	The contents of the Look-Up Tables

The registers/memories are discussed in more detail in the next sections. The tables show the bit assignments, whether they are readable or writeable and what they are reset to.

6.1 Serial Number Register (SERNO)

Bit	Name	Read	Write	Reset to	Description
31:24	SERNO			unaffected	Serial number of the board (unique).
23:17	–			unaffected	Read as zero.
16	PC_TYPE			unaffected	Reads as '1' to identify this PC as untriggered.
15:0	LOCATION			unaffected	DIP switches on PC set to indicate the board's position in the system.

6.2 Control Register (CTRL)

Bit	Name	Read	Write	Reset to	Description
31	ENC			0	FLINK C enable
30	DINC			unaffected	Offset C data in
29	CLKC			unaffected	Offset C clock
28	DOUTC			unaffected	Offset C data out
27	ENB			0	FLINK B enable
26	DINB			unaffected	Offset B data in
25	CLKB			unaffected	Offset B clock
24	DOUTB			unaffected	Offset B data out
23	ENA			0	FLINK A enable
22	DINA			unaffected	Offset A data in
21	CLKA			unaffected	Offset A clock
20	DOUTA			unaffected	Offset A data out
19	LUTEN			0	Specify whether LUTs are accessible from i960 ('1') or are performing data correction ('0').
18	ISEN			0	Specify whether the IS is being reset ('0') or operating as described ('1').
17	SWTRIGEN			0	Specify whether the software trigger to the gate controller is enabled ('1') or disabled ('0').
16:7	SAMPLES			unaffected	Samples per L1A
6:0	DEPTH			unaffected	Depth of presample buffer in samples.

The enable signal for each FLINK (EN_x) controls whether a) the status signals from each FLINK are sent to the CC or gated off and b) whether the CC interface expects address/status from this FLINK when RX_DATA is asserted. If EN_x is '1' then the FLINK is enabled into both these functions.

The sixteen bit offset to be subtracted from LUT data is loaded LSB first into the device that uses it in the same manner as a shift register: there is data in and clock for loading and data from the other end of the shift register appears at data out.

When the ISEN bit changes from '0' to '1' the IS carries out whatever initialisation is required. Changing of most of the parameters in the control register should only be carried out when the IS is disabled.

6.3 Link Status Register (LINK_STAT)

Bit	Name	Read	Write	Reset to	Description
31:22	–			unaffected	Read as zero.
21	ADIN			unaffected	ADC Din
20	ACLK			unaffected	ADC CLOCK
19	ACS*			unaffected	ADC CS*
18	ADOUT			unaffected	ADC DOUT
17	ASSTRB			unaffected	ADC SSTRB
16:15	–			unaffected	Read as zero.
11	RXDETC			unaffected	High when the receiver Finisar for FLINK C detects light from the fibre.
10	LRDYC			0	FLINK C link ready
9:8	LSTC			0	FLINK C start-up state machine state
7	RXDETB			unaffected	High when the receiver Finisar for FLINK B detects light from the fibre.
6	LRDYB			0	FLINK B link ready
5:4	LSTB			0	FLINK B start-up state machine state
3	RXDETA			unaffected	High when the receiver Finisar for FLINK A detects light from the fibre.
2	LRDYA			0	FLINK A link ready
1:0	LSTA			0	FLINK A start-up state machine state

Some analogue quantities are connected to an eight-channel ADC (a MAX192 from Maxim). The software uses the bits labelled ‘ADC *’ to configure it and return the data. See the device data sheet for a description of how to operate it. The quantities available for digitisation are:

Input Number	Description
0	FLINK A received optical power (scale TBD)
1	FLINK B received optical power (scale TBD)
2	FLINK C received optical power (scale TBD)
3	Output of the +5V regulator for the Finisar, divided by two.
4	Output of the –2V regulator, multiplied by –1.
5	unused
6	unused
7	unused

6.4 Trigger Control Register (TRIGCTRL)

Bit	Name	Read	Write	Reset to	Description
31:5	–			unaffected	Read as zero.
4	TRIGTEST			0	Selects whether energy (0) or test pattern (1) is sent to trigger.
3:0	FROFFSET			unaffected	Offset of frame from SYNC

6.5 Software Trigger Register (SWTRIG)

Accessing this register will cause the gate controllers to behave as if they have seen the T_r bit set. This function can be disabled during normal data-taking by a bit in the control register.

6.6 Look-Up-Tables (LUT)

The LUTs are directly mapped onto the i960 bus so random access is possible, when the LUTEN bit in the control register is '1'.

The address field used to access the LUT for each FLINK is broken up as follows:

Bits	Meaning		Description
20:19	FLINK number	0	FLINK A
		1	FLINK B
		2	FLINK C
		3	undefined
18:14	Crystal number	0 – 23	Crystal number
		24 – 31	undefined
13:12	Range bit	0	x1 range
		1	x4 range
		2	x32 range
		3	x256 range
11:2	ADC value	0 – 1023	ADC value

To each defined location in the LUTs the corresponding corrected energy and FEX/ADD bits should be written. The format of the data word is as shown below:

Bit	Name	Read	Write	Reset to	Description
31:18	–			unaffected	Read as zero.
17	ADD			unaffected	The ADD threshold bit
16	FEX			unaffected	The FEX threshold bit
15:0	ENERGY			unaffected	The corrected energy

7. INTERMEDIATE STORE

The Intermediate Store is located at its own base address, the eight most significant (31:24) of which are set by a DIP switch on the PC. The module will only respond correctly to bus accesses that assume a thirty-two bit wide bus, although the byte enables will be used to provide byte-wide addressing. Infinite length burst accesses are supported.

In the prototype each IS will be 8k, sixty-four bit words deep.

Bits	Meaning	Description
18:17	FLINK select	0 FLINK A
		1 FLINK B
		2 FLINK C
		3 undefined
16	–	Undecoded, so that the intermediate store appears twice in the memory map in consecutive locations.
15:3	Offset	Offset within IS.
2	Word select	Select between most significant 32 bits ('1') or least significant ('0') of the sixty-four bit words.

8. CONNECTORS

The UPC has the following connectors

- Two five row DIN41612 connectors to the CC. The pinout for these is given in the CC description, but note that the pin numbers on the connectors we will use will be reversed on the PC and CC. That is to say, pin 1A on the CC will plug into pin 32A on the PC.
- PMC connector. This is an eighty way IDC connector to the cable to the PMC. The pinout is given in the PMC description
- CPU extender. This is a 20 pin IDC that connects LEDs and switches on the front-panel of the PC to the corresponding controls on the CPU. *Where are these pins defined?*
- The connector to the Calorimeter Trigger. *Where is it defined?*

9. FRONT-PANEL

The front-panel for the untriggered PC is described in detail in the DataFlow Platform Users Guide. A summary is given below:

The following LEDs and switches are connected to a cable from the CPU board:

LED Name	Colour	Description
VME	Green	Activity on VME
CPU	Green	Activity on CPU
PCI	Green	Activity on PCI
prog1-4	2 green, 2 red	Programmable LEDs
abort, reset	—	Push buttons

The following LEDs are connected to signals from the CC:

LED Name	Colour – Purpose	Description
Missing Clock	red – error	Lit when SYSCLK is missing.
Internal Clock	yellow – warning	Lit when the CC is running from its internal clock (i.e. not the FCDDM).
CMD	green – advisory	Lit when a command is received on FCDDATA or simulated by the switch unit.
FULL	yellow – warning	Lit when the FULL signal is asserted to the FCDDM.

The following LEDs are driven by the PC, stretched to catch short pulses:

LED Name	Colour – Purpose	Description
i960	green – advisory	Lit when there is activity on the i960 bus
CLINK	green – advisory	Lit when there is a command on the CLINK from the CC
FLINK A,B,C not ready	red – error	Lit when the corresponding FLINK is not ready.

10. RELATED DOCUMENTS

1. J. Dowdell et. al., *BaBar EMC DAQ, IOB Description*
2. J. Dowdell et. al., *BaBar DAQ, Controller Card Description*
3. M. Huffer et. al., *The DataFlow Platform Users Guide*
4. G. Haller et. al., *DAQ Readout Module – Overview*
5. J. Dowdell et. al., *Architecture of the BaBar DAQ Read-Out Module*
6. G. Oxoby, *PCI Mezzanine Card*
7. G. Haller et. al., *Architecture for the BaBar Triggered Personality Card*