

BaBar Calorimeter DAQ I/O Board Description

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1. INTRODUCTION

This document describes the I/O board of the BaBar Electromagnetic Calorimeter (EMC) Data Acquisition (DAQ) system. Different versions of this module will be required for the barrel and end-cap of the detector.

The differences between barrel and end-cap boards are:

- Barrel I/O boards connect to six ADC boards, end-cap I/O boards connect to four ADC boards. This means there are three DAQ fibres from a barrel board but only two from an end-cap board. The fast control registers on the two missing ADC boards will also be missing on end-cap boards.
- the two types are a different size and orientation, although the layouts should be as similar as possible.

The differences are therefore essentially cosmetic, so this document will refer to both sorts of I/O board simply as an IOB.

CONTENTS

1. INTRODUCTION.....	2
2. REVISION HISTORY.....	3
3. CONTROL OF THE ADC AND I/O BOARDS	4
3.1 CLOCK DIVISION.....	4
3.2 THE GLOBAL FAST CONTROL COMMANDS	5
3.3 FAST CONTROL REGISTER ACCESSES.....	5
3.4 THE PROTOCOL RECEIVER.....	7
3.5 PROGRAMMING THE CONTROLLER.....	8
4. DATA TRANSMISSION OFF-DETECTOR.....	9
5. CALIBRATION SIGNAL DISTRIBUTION.....	11
5.1 WHAT THE PRE-AMPLIFIER BOARD EXPECTS.....	11
5.2 THE GRANULARITY OF THE CALIBRATION SIGNALS.....	11
6. POWER DISTRIBUTION.....	13
7. ENVIRONMENTAL MONITORING FUNCTIONS.....	14
7.1 MONITORING THE FINISAR TRANSMITTERS.....	15
7.2 MONITORING ANALOGUE VOLTAGES.....	15
7.3 MONITORING OF G-LINK PLL STATUS.....	16
7.4 READING THE IOB SERIAL NUMBER	16
7.5 THE ELINK.....	17
8. PIN-OUT OF CONNECTORS.....	22
9. PHYSICAL LAYOUT.....	23

 FIGURES

FIGURE 1 — CHECKING THE SYNCHRONISATION OF THE CLOCK DIVIDERS.....	4
FIGURE 2 — FAST CONTROL REGISTERS AT THE FRONT-END.....	7
FIGURE 3 — DATA FORMATTING FOR THE G-LINK.....	9
FIGURE 4 — ADC DATA PACKET FORMAT.....	10
FIGURE 5 — COMBINED CALIBRATION VOLTAGE AND STROBE.....	11
FIGURE 6 — CALIBRATION SIGNAL GENERATION.....	12
FIGURE 7 — THE CALIBRATION DAC REGISTER.....	12
FIGURE 8 — CALIBRATION CONTROL REGISTER.....	12
FIGURE 9 — POWER DISTRIBUTION ON THE IOB.....	13
FIGURE 10 — BLOCK DIAGRAM OF ENVIRONMENTAL MONITORING ON THE IOB.....	14
FIGURE 11 — SIGNALLING STANDARD OF THE E-LINK.....	17
FIGURE 12 — TOP SIDE OF THE END-CAP I/O BOARD.....	23
FIGURE 13 — BOTTOM SIDE OF THE END-CAP I/O BOARD.....	24
FIGURE 14 — B-IOB PRELIMINARY LAYOUT.....	25

2. REVISION HISTORY

Date Issued	Description of Revisions
24-Mar-97	<ul style="list-style-type: none"> Changes for pre-production (extra CARE register, AC coupled cal strobe, add CLKOV, remove VDIODE)

3. CONTROL OF THE ADC AND I/O BOARDS

All clock and control information is received in the form of the C-LINK and D-LINK via the transition board, in electrical form.

There is therefore a cable between the transition board and IOB that carries:

- C-LINK data (59.5 Mbit/s) from transition board to IOB
- system clock (59.5 MHz) from transition board to IOB
- D-LINK data (59.5 Mbit/s) from IOB to transition board
- return clock (59.5 MHz) from IOB to transition board

The return clock is simply a copy of the received system clock. The transition board uses it to drive the return G-LINK, this means that the system is self-synchronising if the cable lengths from transition boards to IOBs are identical.

3.1 Clock Division

The only clock distributed to the IOB is the 59.5MHz system clock. From this the following clocks are derived using a clock divider:

- `SAMPLE` — the sample clock to the CARE. This clock is always 3.7MHz (one sixteenth the system clock).
- `DIGITISE` — the digitise clock to the ADCs. This clock will be either 3.7MHz or 14.9MHz (one quarter the system clock). Which of the two frequencies is used is set by a bit in a control register.

The clock divider is implemented as a sixteen state, state machine. It is therefore controlled by a four bit state register (this state register appears basically as a four bit binary counter).

As every I/O board has its own state register they must all be kept synchronised. The mechanism for doing this is the SYNC strobe from fast control, which resets the state register to zero. This strobe should arrive at all IOBs at the same time so all counters should then be synchronised.

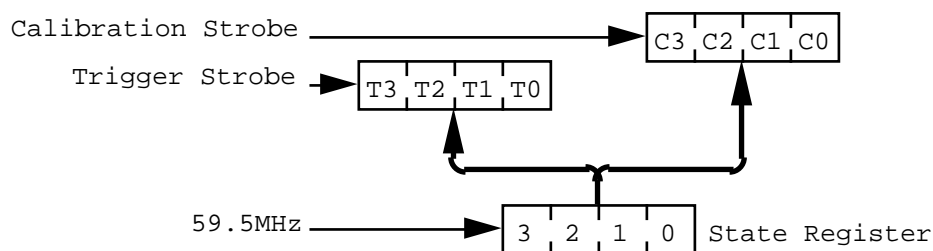


Figure 1 — Checking the synchronisation of the clock dividers

We must then continue to check that the counters are synchronised, and issue another SYNC strobe when necessary. The mechanism for doing this is illustrated in Figure 1. When a trigger strobe is decoded by the protocol receiver it latches the contents of the clock divider into another register (T[3:0]). The T[3:0] bits are sent to the DAQ boards in the packets containing ADC data, so synchronisation can be checked by comparing the T[3:0] bits for all IOBs on the detector.

In the same way, the contents of the clock divider are latched in the register C[3:0] when a calibration strobe is decoded, and sent to the DAQ cards in the same way. This can also be used to check synchronisation, and as a check of the phase of the calibration strobe with respect to the sample clock.

3.2 The Global Fast Control Commands

“Global Fast Control Commands” represent ‘strokes’ from the fast control system and are used to control data taking. The format for these commands is (time flowing to the right):

0	1	C0	C1	C2	C3	C4	D0	D1	D2	D3	D4
---	---	----	----	----	----	----	----	----	----	----	----

Where C0...C4 are command bits that give the opcode of the operation that is to be performed and D0...D4 are data bits. Commands can come back-to-back, therefore we are only guaranteed one zero between the end of the previous packet and the start bit of the next.

Opcode	Command	Data	Action taken by the protocol receiver upon decoding the strobe
0x0	No Op	0	Take no action.
0x1	Clear Readout	reserved	Take no action.
0x2	SYNC	reserved	Synchronous reset of the clock divider.
0x3	Level 1 Trigger Accept	Trigger Tag	Sample the state register of the clock divider. Ignore the trigger tag.
0x4	Read Event	Trigger Tag	Take no action.
0x5	Calibration Strobe	reserved	Sample the state register of the clock divider. Assert the calibration strobe to the preamps. De-assert it 500 μ s later.

3.3 Fast Control Register Accesses

Several control registers exist at the front-end to control the CARE chips, the calibration and other things. These registers are written into via the C-LINK in the same way as fast control strobes are sent. The format for these commands is (time flowing to the right, then down):

0	1	C0	C1	C2	C3	C4	A0	A1	A2	A3	A4				
D0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
D1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
...															

Where C0...C4 are command bits that give the opcode of the operation that is to be performed, A0...A4 are address bits and D0, D1... are data bits. In principle the data bits following the command code and address are sent at 59.5Mbit/s, however for reasons that will be explained in the section on the protocol receiver the registers can only accept data at a much slower rate. Therefore only every sixteenth data bit is written into the registers, this reduces the data rate to 3.7Mbit/s. The number of data bits is fixed for each command code, but varies from code to code.

The write operations are listed below, any commands not listed are treated as a No-op. The bit assignments in these registers are described elsewhere.

Opcode	Command	Address (hex)	Action by the protocol receiver
0x1F	reserved	ignored	Reserved, treat as No-op.
0x1E	local reset	ignored	Unused.
0x1D	Write CARE control (override & diode select)	0...6	Write CARE chip control register number 0...6.
0x1C	Write CAL control (enables & capacitor selects)	ignored	Write calibration control register.
0x1B	Write CAL DAC	ignored	Write calibration DAC value.
0x1A	Write control reg.	ignored	Write into the control register.

Read operations exist one-for-one with the above write operations, except for the calibration DAC. They are formatted exactly as write operations, but the command codes are one of those in the table below and there is no data following them. When the protocol receiver decodes a read operation it must retrieve the value from the register and send a response packet back to the DAQ board.

That response consists of a sixteen bit header and data from the register. Again the data rate from the registers is reduced to 3.7Mbit/s by making only every sixteenth data bit significant. The response packet is shown below (time flowing to the right and down):

1	?	REG (1)	C0	C1	C2	C3	C4	A0	A1	A2	A3	A4	?	?	?
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	D0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	D1
...															

Where 'REG' is the bit in other systems that distinguishes register readback data from event data. Since we only have register readback data this bit is always a '1'. The C0...C4 and A0...A4 bits are the same as those in the read request that generated this packet. Bits marked with '?' are undefined and should be sent as '0' for now.

The opcodes of readback commands are:

Opcode	Command	Address (hex)	Action by the protocol receiver
0x19	Read CARE control (override & diode select)	0...6	Read the CARE control register number 0...6.
0x18	Read CAL control (enables & capacitor selects)	ignored	Read calibration control register.
0x17	No-op	ignored	Read calibration DAC is not possible.
0x16	Read control reg.	ignored	Read from the control register.

3.4 The Protocol Receiver

A protocol receiver “device” on the IOB decodes the serial data stream and controls the rest of the electronics on the I/O and ADC boards.

When there is no command the C-LINK is ‘0’, the start of a packet is indicated by a start bit (‘1’). Packets can start on any 59.5MHz boundary. This allows the trigger and calibration strobe to be asserted in 16ns increments.

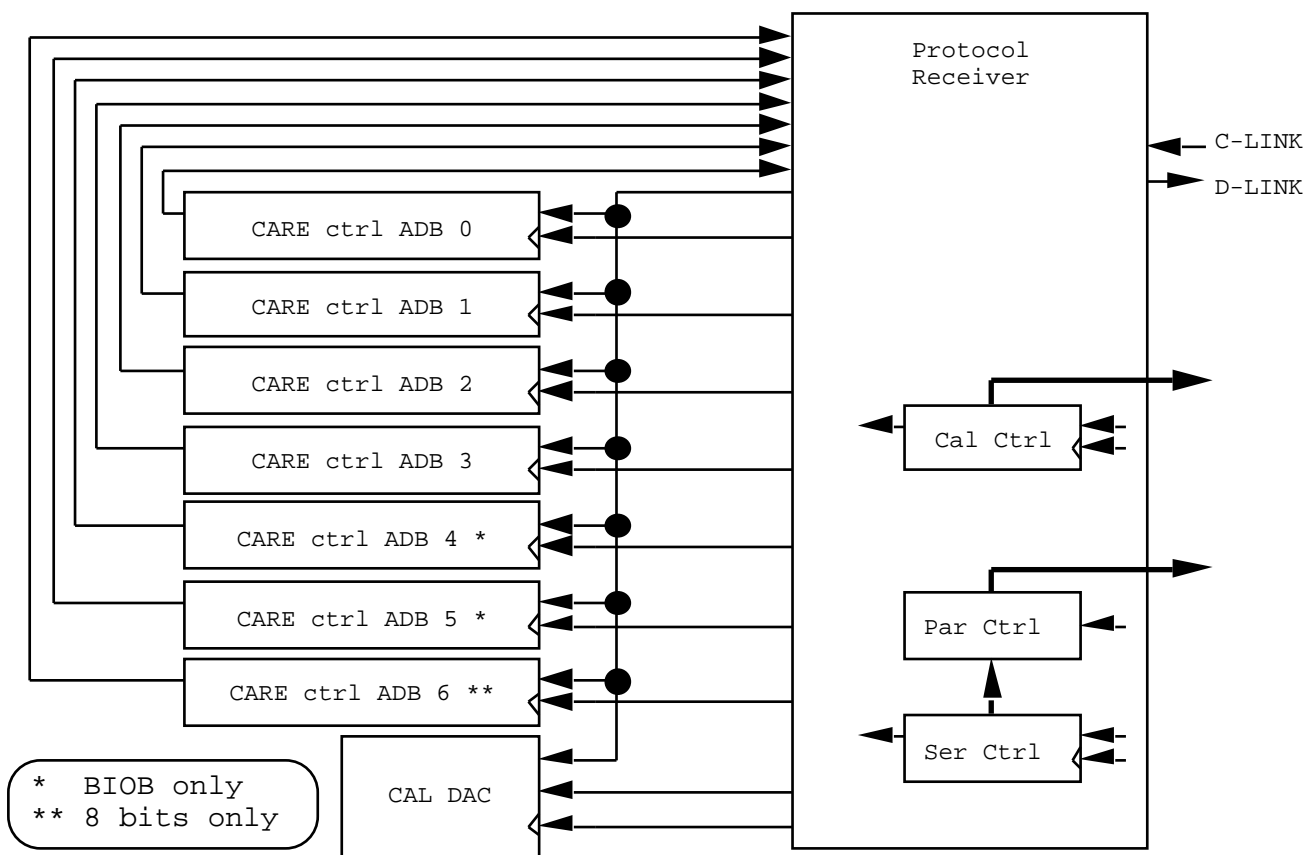


Figure 2 — Fast Control Registers at the front-end

The fast control registers are implemented as shown in Figure 2.

- The CARE control registers are implemented as simple shift registers inside the CARE chips on the ADB. One register per ADB. The interface to this consists of data in, data out and clock. CARE register number 6 is implemented primarily as a test feature.
- The calibration DAC register is implemented inside the DAC itself and cannot be read back. The interface to this is a clock, data and chip enable.
- The calibration control register is implemented inside the PLD with the protocol receiver as a simple shift register.
- The control register is implemented inside the PLD as a combination of serial and parallel register. Data to be written is shifted into the serial register and then parallel loaded into the parallel register. Readback occurs from the serial register. This is necessary to ensure the control signals do not see shifting data.

For those registers that are implemented as shift registers: the protocol receiver automatically loops the output data back to the input so the register is left with the same contents as it started with after a read.

The external registers cannot be written into at 59.5Mbit/s, hence the reduction of the data rate to 3.7 Mbit/s described earlier. All registers are written into at the same rate for simplicity.

The control register on the I/O board is shown below:

Bit	Name		Description
0	LINK_ENABLE	0	Switch the DAQ links to idle (send fill frames)
		1	Send formatted data packets to DAQ.
1	LINKTEST	0	ADBs run normally
		1	The ADBs drive a known repeating pattern up the fibre
2	DCLKSEL	0	DIGITISE clock runs at 14.9 MHz
		1	DIGITISE clock runs at 3.7 MHz
3	FIN_RESET*	0	Reset the Finisar transmitters to the DAQ system.
		1	Finisar transmitters to DAQ function normally.
4	FIN_OFF	0	Turn on the laser in the Finisar transmitters to the DAQ system
		1	Turn off the laser.
5	GLINK_RESET*	0	Reset the G-LINK transmitters to the DAQ system.
		1	G-LINK transmitters to DAQ function normally.
6	SERNOSEL	0	Send CLINK packet header in FLINK bits 18,19
		1	Send serial/fibre number in FLINK bits 18, 19
7	—		

3.5 Programming the Controller

All control functions on the IOB are integrated into a single programmable logic device. This device stores its configuration in electronically erasable memory, so the configuration is non-volatile but can be changed. Programming the device (setting its configuration) is done in-system via an industry standard test access bus (JTAG) from a PC. This will allow it to be programmed after board assembly (during testing) and reprogrammed while still plugged into the detector.

The functions of the devices should be fixed, so such reprogramming will be done rarely. There is a connector on the IOB to accept a programming cable from a PC, however since this facility will not normally be used there will be no cable running off-detector.

4. DATA TRANSMISSION OFF-DETECTOR

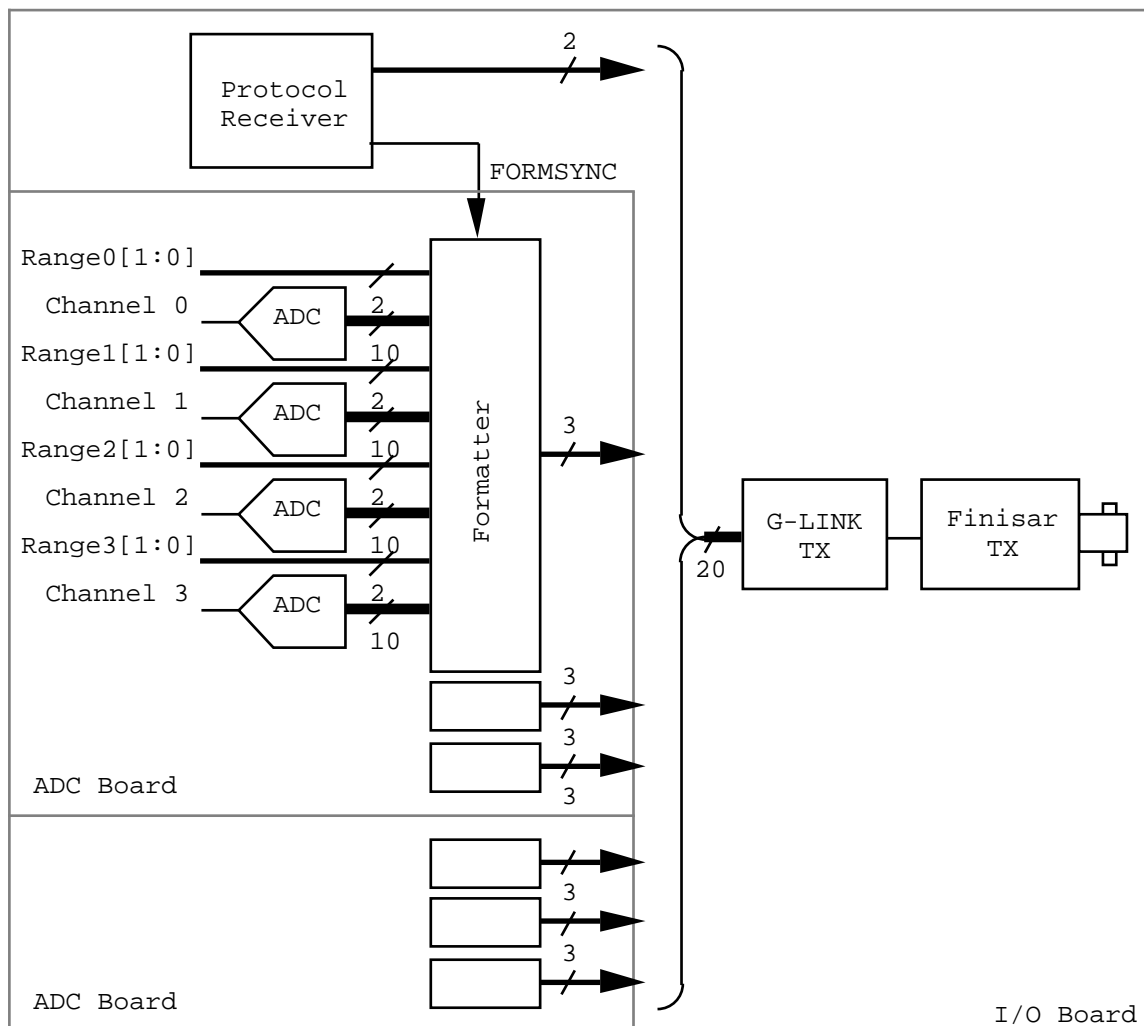


Figure 3 — Data formatting for the G-LINK

A block diagram of the process of formatting the ADC data for the G-LINK to DAQ (referred to as an FLINK) is shown in Figure 3. Essentially the data sampled by the CARE and ADC chips in each 3.7 MHz sampling cycle is sent in packet format down the G-LINK to the DAQ board.

Each CARE is followed by a data formatter which takes the 48 bits from the CAREs and ADCs at 3.7MHz and transforms them into three bits at 59.5 MHz. The formatters from two ADC boards are concatenated into one G-LINK (hence 24 crystals per G-LINK).

The protocol receiver controls the data formatters on the ADC board and the G-LINK transmitter. It also adds two bits of control information to the packet.

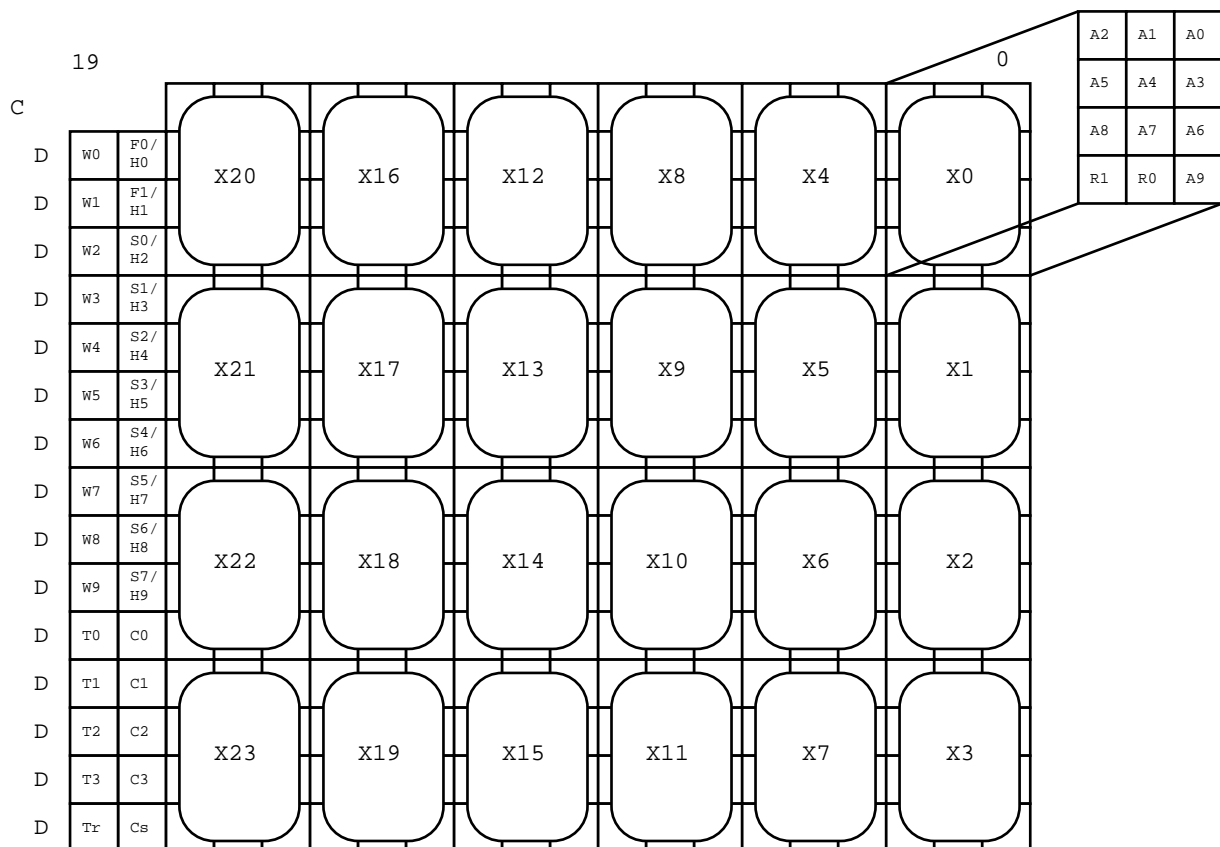


Figure 4 — ADC data packet format

Figure 4 shows the format of the data packet sent down the G-LINK to the DAQ board. The meaning of the bits is shown below:

- X0...X23 represent one sample per crystal. Inside each sample R1, R0 are the range bits and A9...A0 is the ADC output.
- Some of the bits in bit 18 can be programmed (via SERNOSEL in the control register) to be either:
 - 1) S7...S0 is the serial number of the I/O board that the fibre originated from. F1...F0 is the number of the fibre (1 to 3) on that I/O board. These two quantities together uniquely identify the source of the data.
 - 2) The ten bits [H9...H0] contain the header of the last command sent down the CLINK. This is the standard mode for data taking and allows the trigger tag from the L1Accept to be associated with the data.
- W9...W0 represents a nine bit time counter (also called a 'wall clock') clocked at 3.7 MHz.
- T3...T0 represent the state of the clock divider the last time a trigger was received and Tr is '1' if a trigger was received during the previous sample period.
- C3...C0 represent the state of the clock divider the last time a calibration strobe was received and Cs is '1' if a calibration strobe was received during the previous sample period.

5. CALIBRATION SIGNAL DISTRIBUTION

5.1 What the pre-amplifier board expects

Electronics calibration uses the following signals:

- a calibration voltage
- a calibration strobe, and
- a calibration capacitor select.

When the calibration strobe is asserted an amount of charge proportional to the calibration voltage is injected via a capacitor into the input of the pre-amp. One of two different valued capacitors can be used for this injection (controlled by the calibration capacitor select), giving two ranges.

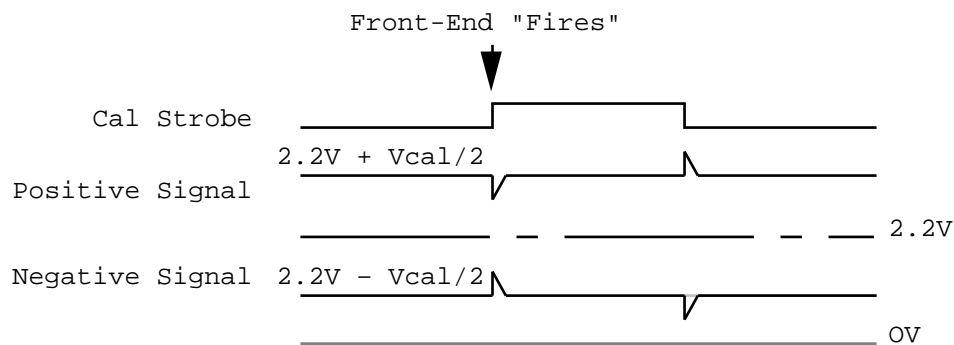


Figure 5 — Combined calibration voltage and strobe

The capacitor select is transmitted to the pre-amp as a CMOS level.

To save pins, the calibration voltage and strobe are combined into one differential pair as shown in Figure 5. The calibration voltage corresponds to the difference between the positive and negative signals. The calibration strobe is a differential signal AC coupled on top of this. There is a filter with a time constant of about 1ms between the calibration voltage input on the pre-amp chip and the actual calibration capacitor in order to reduce the effect of the strobe on the charge injected. The strobe is asserted for 500 μ s following a receipt of a fast control calibration strobe command.

5.2 The granularity of the calibration signals

Nice though it would be to be able to pulse each pre-amp individually, we do not have enough space on the boards to generate that many calibration signals. Instead several pre-amps are driven by the same calibration signals.

The calibration command is carried on the C-LINK therefore its distribution can be controlled at the granularity of I/O boards. Note: the calibration command from the fast control indicates only when the calibration strobe is to be asserted; the protocol receiver automatically de-asserts the calibration strobe 500 μ s later.

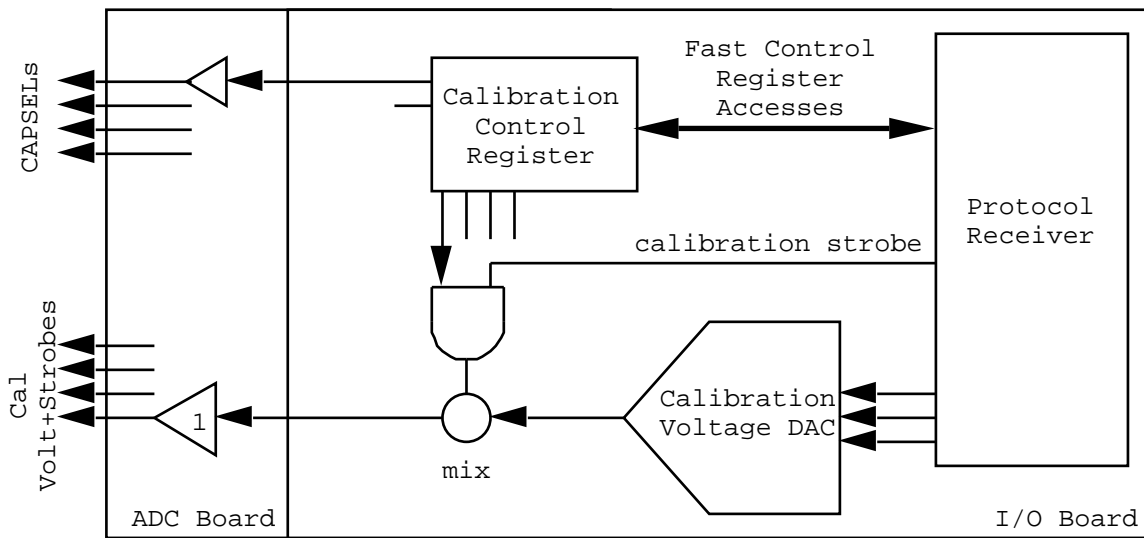


Figure 6 — Calibration signal generation

The calibration voltage is generated by a sixteen bit DAC on the I/O board, as shown in Figure 6. It is therefore common to all the pre-amps connected to that I/O board.

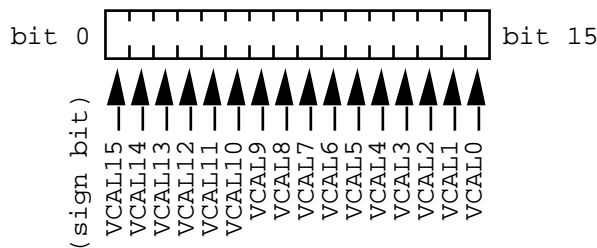


Figure 7 — The calibration DAC register

Figure 7 shows the bit assignment in the calibration DAC register. It is in two's complement signed format, with the MSB shifted in first (bit 0 in fast control parlance).

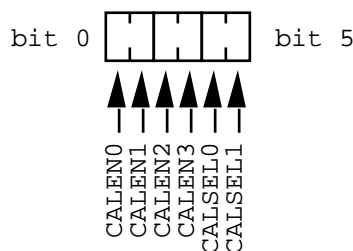


Figure 8 — Calibration Control Register

Two capacitor selects and four strobe enables (which gate the calibration strobe) are stored in the calibration control register on the IOB, as shown in Figure 8.

6. POWER DISTRIBUTION

The power supplies used or passed through the IOB are shown below.

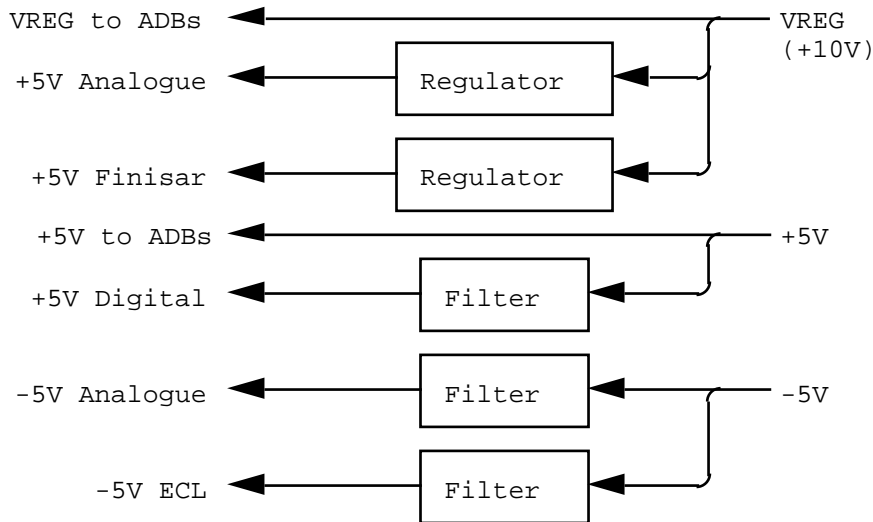


Figure 9 — Power distribution on the IOB

The voltages on the right hand side come from the power supply units to the I/O board. This then processed as shown below:

- VREG (10V) and +5V are sent straight to the ADB.
- +5V Analogue (for the calibration DAC) is derived from VREG via a regulator.
- +5V Finisar (for the Finisar transmitters) is derived from VREG via a regulator. This is because the Finisars are very sensitive to the quality of their supply voltage.
- +5V digital is simply filtered.
- -5V ECL is simply filtered.
- -5V analogue is simply filtered.

The total current consumption per supply for a B-IOB is approximately:

Supply	BIOB (A)	EIOB (A)
VREG (+10V)	0.4	0.3
+5V	1.5	1.5
-5V	2.1	1.6

The total power dissipated on the B-IOB board is of the order of 22W. The E-IOB is missing one G-LINK and one Finisar, hence its power dissipation is of the order of 18.5W.

There will be an electrostatic shielding enclosure over the top of the board (the bottom will be covered by a screen layer and there will be no components on the bottom of the board). This shielding will be connected to the outer shield of the detector. The hot components will be in thermal contact with the screen can, so cooling can be performed by connecting the shield to a cooled surface.

7. ENVIRONMENTAL MONITORING FUNCTIONS

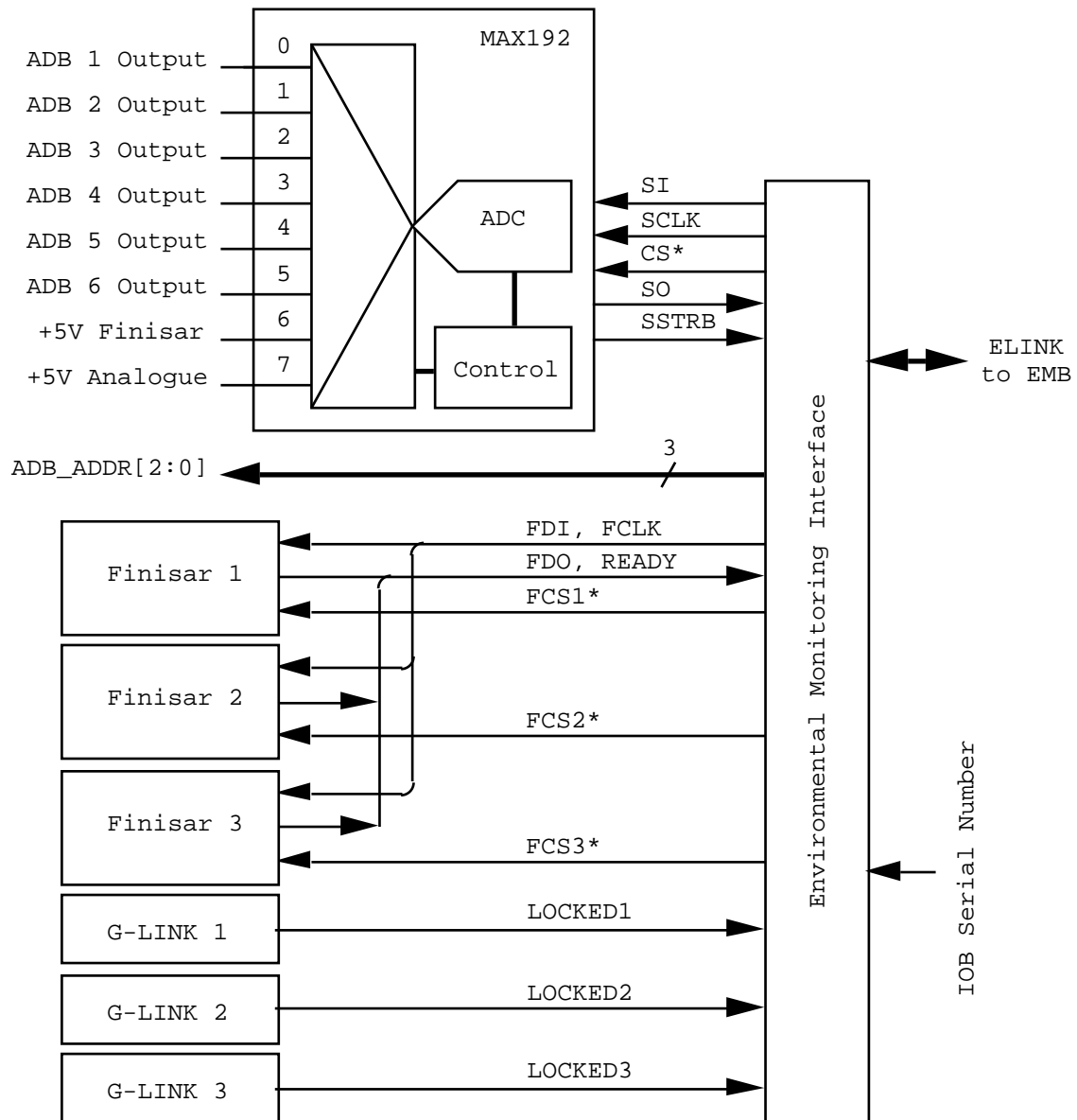


Figure 10 — Block diagram of environmental monitoring on the IOB

A block diagram of the environmental monitoring functions of the IOB is shown in Figure 10. The philosophy is to have an 'Environmental Monitoring Interface' which is accessed from the Environmental Monitoring Board (EMB) via the 'ELINK'. The principle assumption behind what follows is that there is a microcontroller on the EMB controlling all this, therefore the circuitry on the IOB can be made very simple.

7.1 Monitoring the Finisar Transmitters

The three Finisar transmitters each contain a test and diagnostic port that can be used to determine their serial numbers, output power, temperature and so on. The interface is described in detail in Finisar Application Note AN-2010, available from Finisar or viewable on the WWW from the Finisar home page: <http://www.finisar.com>. Suffice to say for now that the Finisar looks like a shift register and the signals involved are:

- DI (bit serial input to the devices)
- DO (bit serial output from the devices, tristate)
- DCLK (bit clock input to the devices)
- READY (handshaking output from the device, open collector)
- CSn* (device select input to each device)

7.2 Monitoring Analogue Voltages

The digitisation of analogue values by the environmental monitoring system is performed by an eight channel ten bit ADC. Six of the inputs are connected to the output of the analogue MUX on the ADBs. The other two connect to the outputs of the two regulators on the IOB (one for the Finisars and one for the analogue components).

The possible inputs and the applied scaling factors (to ensure the input voltages are within the input range of the ADC) are shown below.

MUX address	Description	Expected Voltage	Scale Factor
0	Analogue output of ADB number 0	N/A	1
1	Analogue output of ADB number 1	N/A	1
2	Analogue output of ADB number 2	N/A	1
3	Analogue output of ADB number 3	N/A	1
4	Analogue output of ADB number 4	N/A	1
5	Analogue output of ADB number 5	N/A	1
6	+5V Finisar	5	2
7	+5V Analogue	5	2

The MUXes on the ADBs require a three bit address to select which quantity to connect to the IOB. This address provided directly from the control register and is common to all ADBs.

Just like the Finisar, the ADC looks like a shift register from the control and readout port. This interface is described in detail in the device data sheet (it is a MAX192, manufactured by MAXIM). The signals involved are:

- DIN (bit serial input to the device)
- DOUT (bit serial output from the device)
- SCLK (bit clock to the device)
- CS* (chip select to the device)
- SSTRB (output which indicates when a conversion is in progress)

7.3 Monitoring of G-LINK PLL Status

The Phase Locked Loop (PLL) in each G-LINK transmitter must be in lock for useful data to be transmitted. Fortunately the G-LINK provides a 'LOCKED' signal that indicates whether the PLL is locked (logic '1') or out of lock (logic '0'). This status must be able to be inspected via the ELINK.

The EMB will only be able to inspect the state of the G-LINK infrequently, so it is possible for periods out of lock to go unnoticed unless they are remembered. To this end the EMB can see not only the instantaneous state of the LOCKED signal, but whether it has made a positive transition since the last time the EMB looked.

7.4 Reading the IOB Serial Number

The serial number of the IOB can be determined via the ELINK.

7.5 The ELINK

The philosophy behind the ELINK is very similar to that of the C/D-LINK. Requests for data are sent in a serial format from EMB to IOB and results are sent from IOB to EMB in a serial format. The same serial clock (from the EMB) is used to clock data in both directions.

To minimise problems with ground loops and different power supplies the interface between the EMB and IOB is optically isolated with low voltage swing and edge rates.

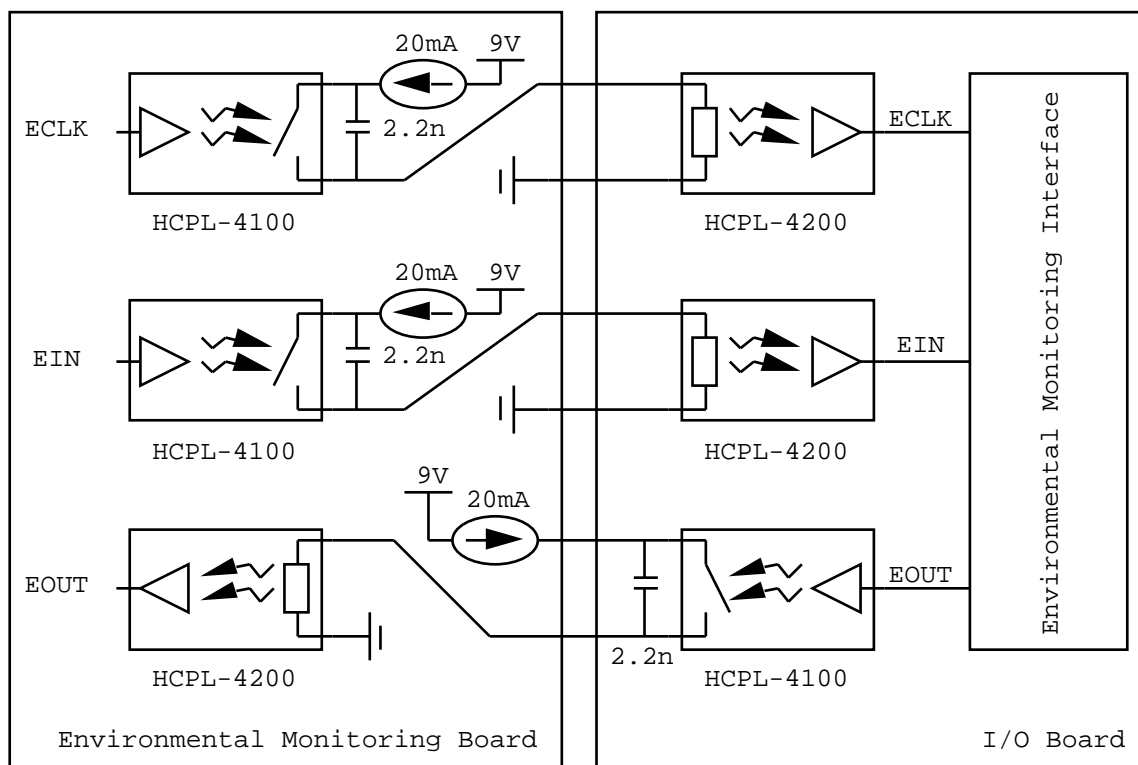


Figure 11 — Signalling Standard of the E-LINK

The E-LINK is implemented using 20mA current loop signalling, as shown in Figure 11. This standard meets the voltage swing and edge rate requirements. The maximum data rate is in excess of 20kbit/s.

The details of the transaction on the ELINK differ from operation to operation, so each will be discussed individually. The exception to this is the 'header'; this is basically an address to specify what sort of transaction will happen next.

The ECLK is implied in the following discussion: transmitting a bit of data from EMB to IOB requires the data to be put on EIN and a positive edge on ECLK. Similarly, data on EOUT is updated on positive edges of ECLK.

7.5.1 Specifying the transaction

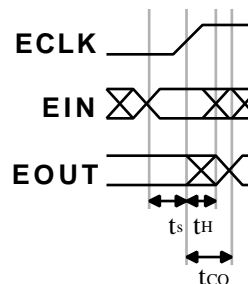
The idle state of both EIN and $EOUT$ is logic '0'. There must be at least one '0' on EIN between transactions (there can be more, or the clock can be stopped). The start of a transaction is indicated by a 'start bit' — a logic '1'. The next six bits to be transferred specify the command code (least significant bit first). This determines which device is being addressed.

0	1	c0	c1	c2	c3	c4	c5
---	---	----	----	----	----	----	----

The following command codes are defined:

c0	c1	c2	c3	c4	c5	Type of transaction
1	0	0	a0	a1	a2	access ADC with ADB MUX address [a0 , a1 , a2]
1	0	1	a0	a1	x	access Finisar number [a0 , a1]
1	1	0	0	x	x	return test pattern
1	1	0	1	x	x	return IOB serial number
1	1	1	x	x	x	return GLINK locked status
0	x	x	x	x	x	invalid. The interface returns to waiting for start bit (this handles the case where a bit error fakes a start bit).

7.5.2 General Mach Timing



set-up time

$$t_s > 5\text{ns}$$

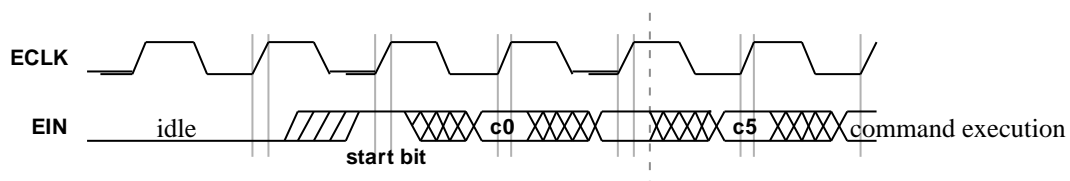
hold time

$$t_H > 5\text{ns}$$

clock rising edge to output delay

$$t_{CO} < 14\text{ns}$$

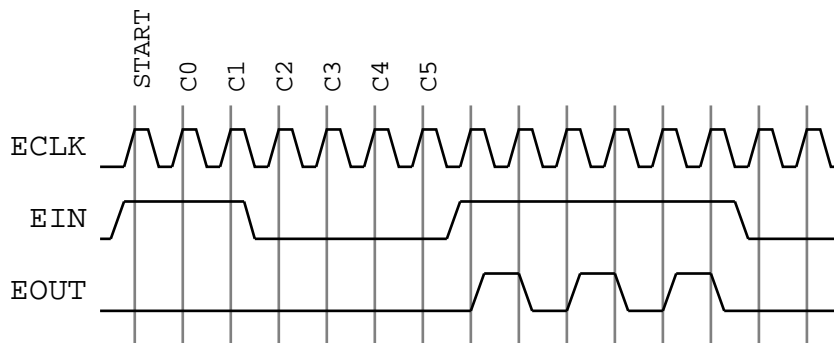
7.5.3 Command Load



The ELINK interface remains idle until a start bit at EIN is detected on the rising edge of $ECLK$. On the rising edges the command of the format c0 c1 c2 c3 c4 c5 is clocked into the interface. If a command is interrupted or completes execution then the interface returns to idle.

7.5.4 Test Signal Output

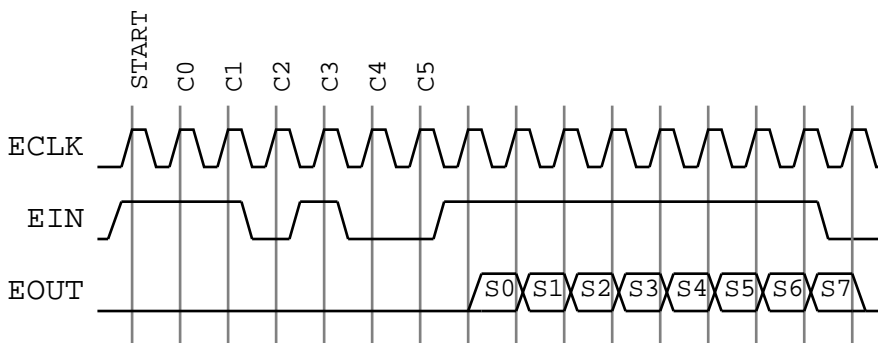
The following diagram shows the timing for this operation. ECLK, EIN, EOUT are the ELINK signals.



After the test signal command has been executed, EOUT toggles on the rising edge of ECLK until EIN goes low.

7.5.5 Serial Number Output

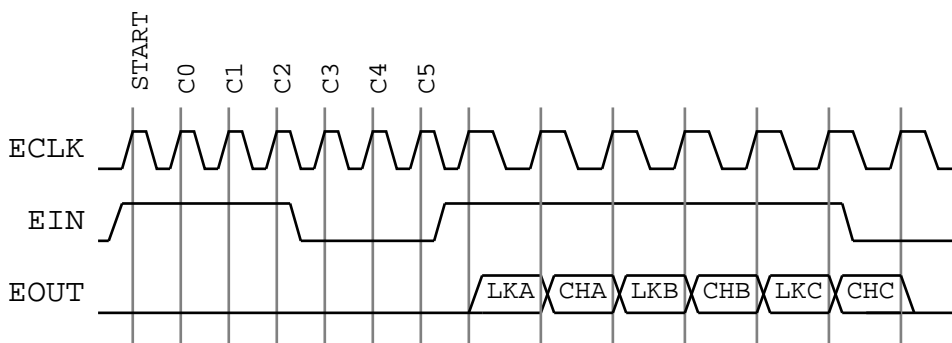
The following diagram shows the timing for this operation. ECLK, EIN, EOUT are the ELINK signals.



When the serial number has been requested the 8 bits will be shifted out LSB first while EIN is high. EIN going low will return the interface to the idle state. The interface will shift out zeroes after the serial number until EIN returns to zero.

7.5.6 GLINK Lock Status Output

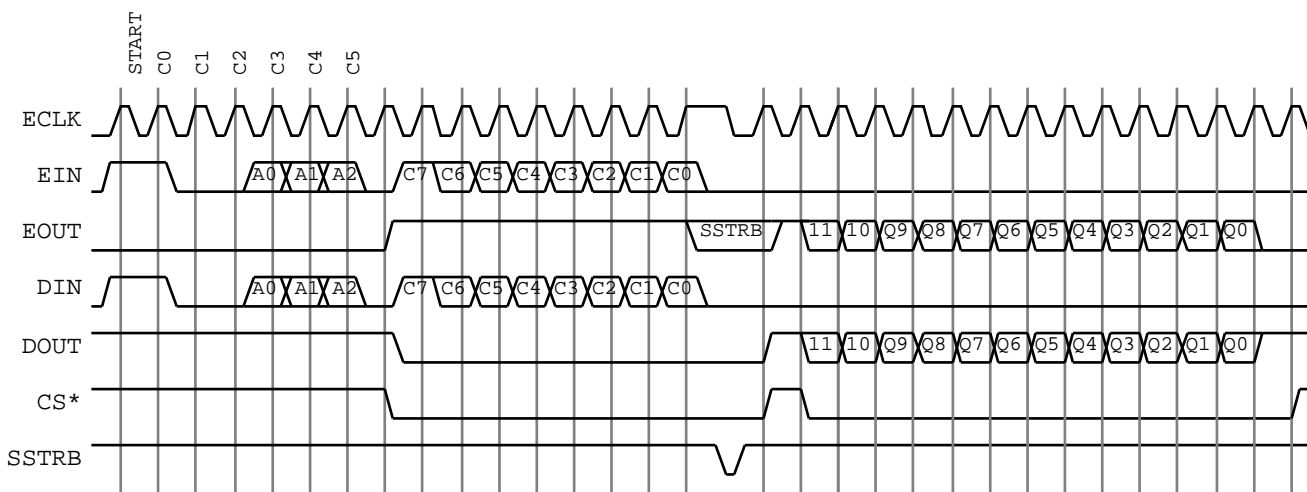
The following diagram shows the timing for this operation. ECLK, EIN, EOUT are the ELINK signals.



While EIN is high the GLINK data will be shifted out in this order glock a, glitch a, glock b, glitch b, glock c, glitch c (where lock is the instantaneous lock value and latch is high if there has been a positive edge on the LOCK signal since the last read). EIN dropping low will return the interface to the idle state. Zeroes will be clocked out after the GLINK data until EIN becomes low.

7.5.7 ADC Timing

The following diagram shows the timing for this operation. ECLK, EIN, EOUT are the ELINK signals. DIN is the data into the ADC, DOUT is data from the ADC, CS* is the chip select to the ADC, SSTRB is the handshaking signal from the ADC.



ADC set-up time > 100ns

ADC hold time > 0ns

delay between falling clock edge and ADC output 20-150ns

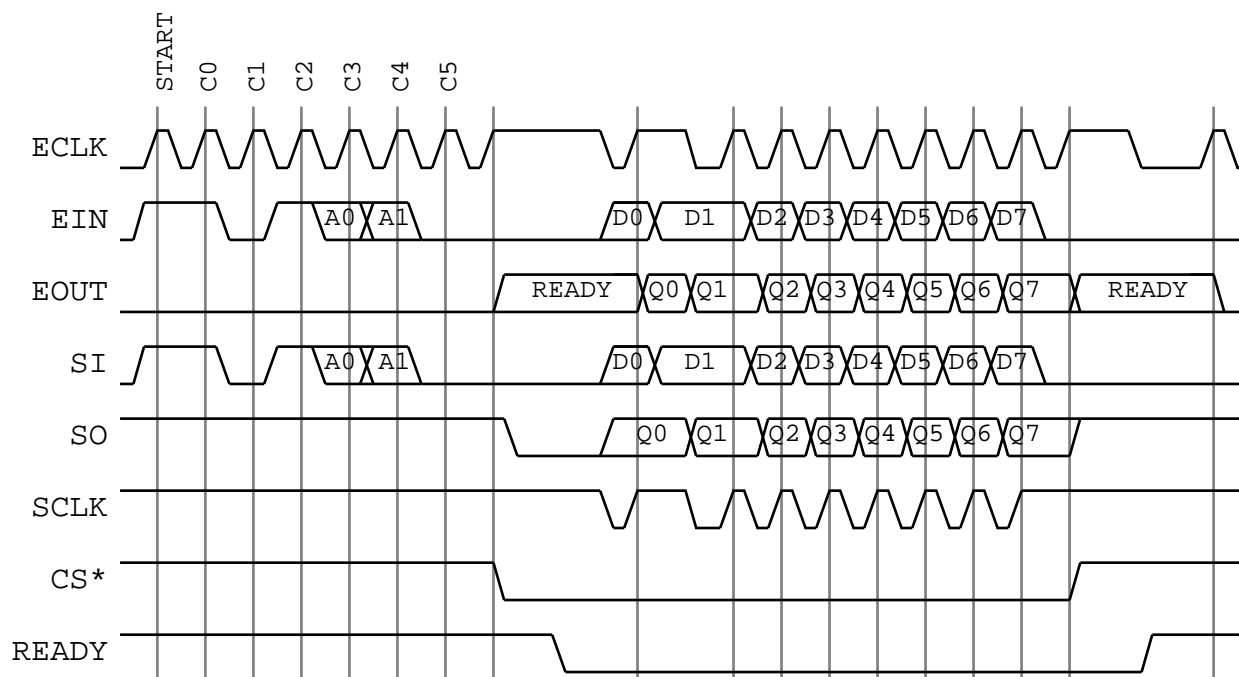
Data is clocked into the ADC on the rising edge of ECLK and is clocked out on the falling edge. During this command execution the AMUX is set with the assigned ADC address.

After eight data bits have been clocked into the ADC, ECLK is to be held high until A_SSTRB (shown on EOUT) pulses low (for approx. 10 μ s). The next falling clock edge with CS \sim low will begin clocking out data from the ADC.

While data is being shifted out, a rising clock edge with EIN high will terminate the conversion and return the interface to the idle state.

7.5.8 Finisar Timing

The following diagram shows the timing for this operation. ECLK, EIN, EOUT are the ELINK signals. SI is data into the Finisar, SO is data out of the Finisar, SCLK is the clock to the Finisar, CS* is the chip select to the Finisar and READY is the handshake signal from the Finisar.



READY goes low after CS \sim asserted	25-1000 μ s
READY tri-state after CS \sim deasserted	100-1000 μ s
Finisar set-up time	> 0.1 μ s
Finisar hold time	> 0.1 μ s
delay between READY low and first clock falling edge	> 0 μ s

When the command is immediately executed ECLK is to be held high until F_READY (shown on EOUT) goes low. A rising edge on ECLK with F_READY high will return the interface to the idle state. After the eight data bits have been clocked out/in ECLK is to be held high until F_READY (shown on EOUT) goes high. The next rising clock pulse returns the interface to idle. Data is clocked into the Finisar on the rising edge of ECLK and clocked out on the falling edge.

8. PIN-OUT OF CONNECTORS

The pin-out of the connector to the ADC board is shown in the ADC board write-up.

The pin-out of the connector to the transition board is shown below. All signals are differential ECL. The connector is a 10 pin surface mount type.

SYSClk in (true)	1	2	SYSClk in (complement)
CLINK data in (true)	3	4	CLINK data in (complement)
SYSClk out (true)	5	6	SYSClk out (complement)
DLINK data out (true)	7	8	DLINK data out (complement)
GND	9	10	GND

The pin-out of the ELINK connector is shown below. The connector is a 6 pin surface mount type.

ECLK+	1	2	ECLK-
EIN+	3	4	EIN-
EOUT+	5	6	EOUT-

Power is supplied to the board through FASTON spades. Sense wires are crimped into the same lug as the supply cable, so they do not appear separately. The connections are:

- VDIODE and its return.
- VREG and its return
- +5V and its return
- -5V and its return
- the two ends of a temperature operated bi-metallic switch. This device is normally closed, opens above 50°C and closes under 30°C. This is used for the temperature interlock.

9. PHYSICAL LAYOUT

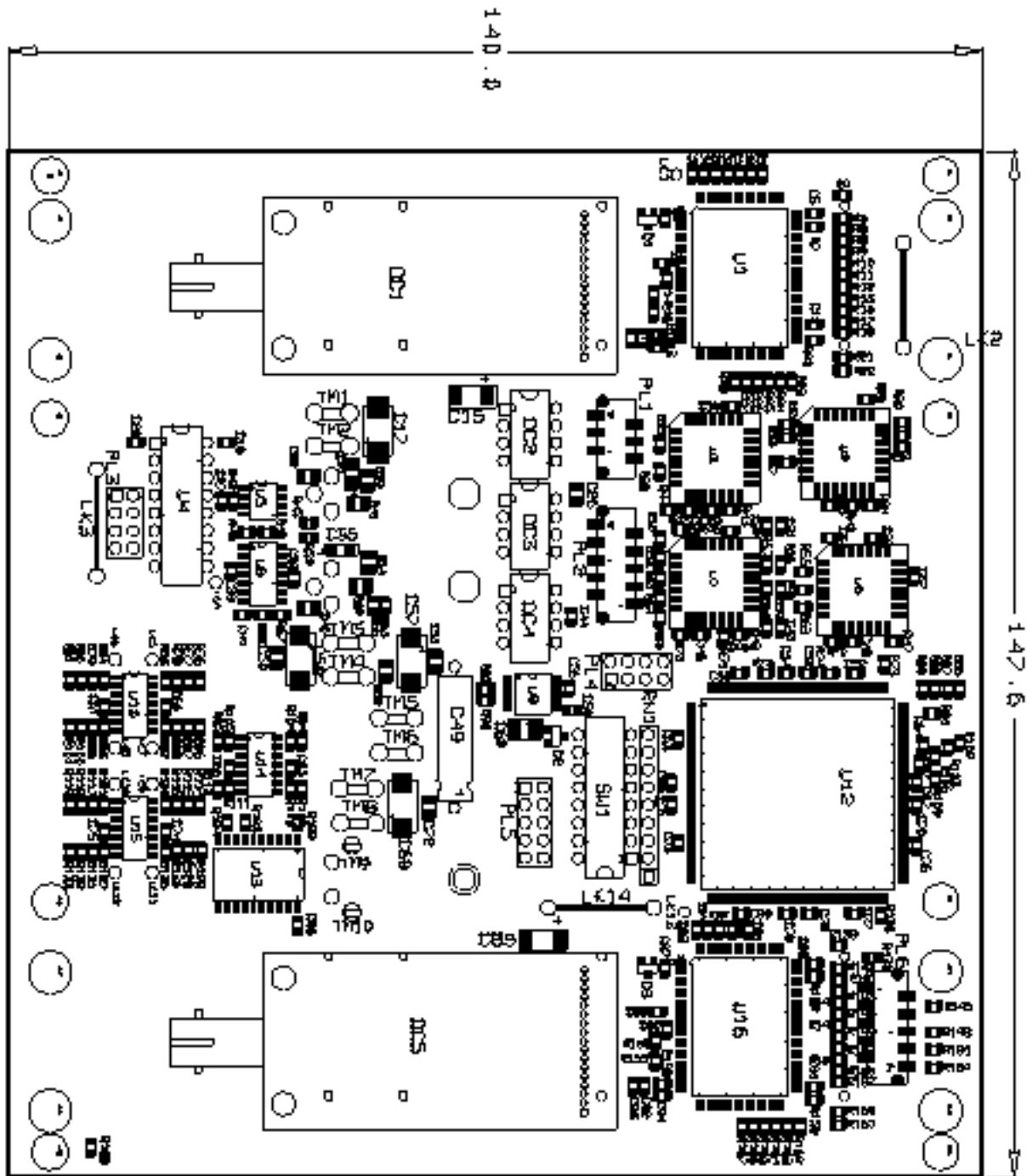


Figure 12 — Top side of the End-Cap I/O Board

The top component layout of the prototype end-cap IOB (E-IOB) is shown in Figure 12.

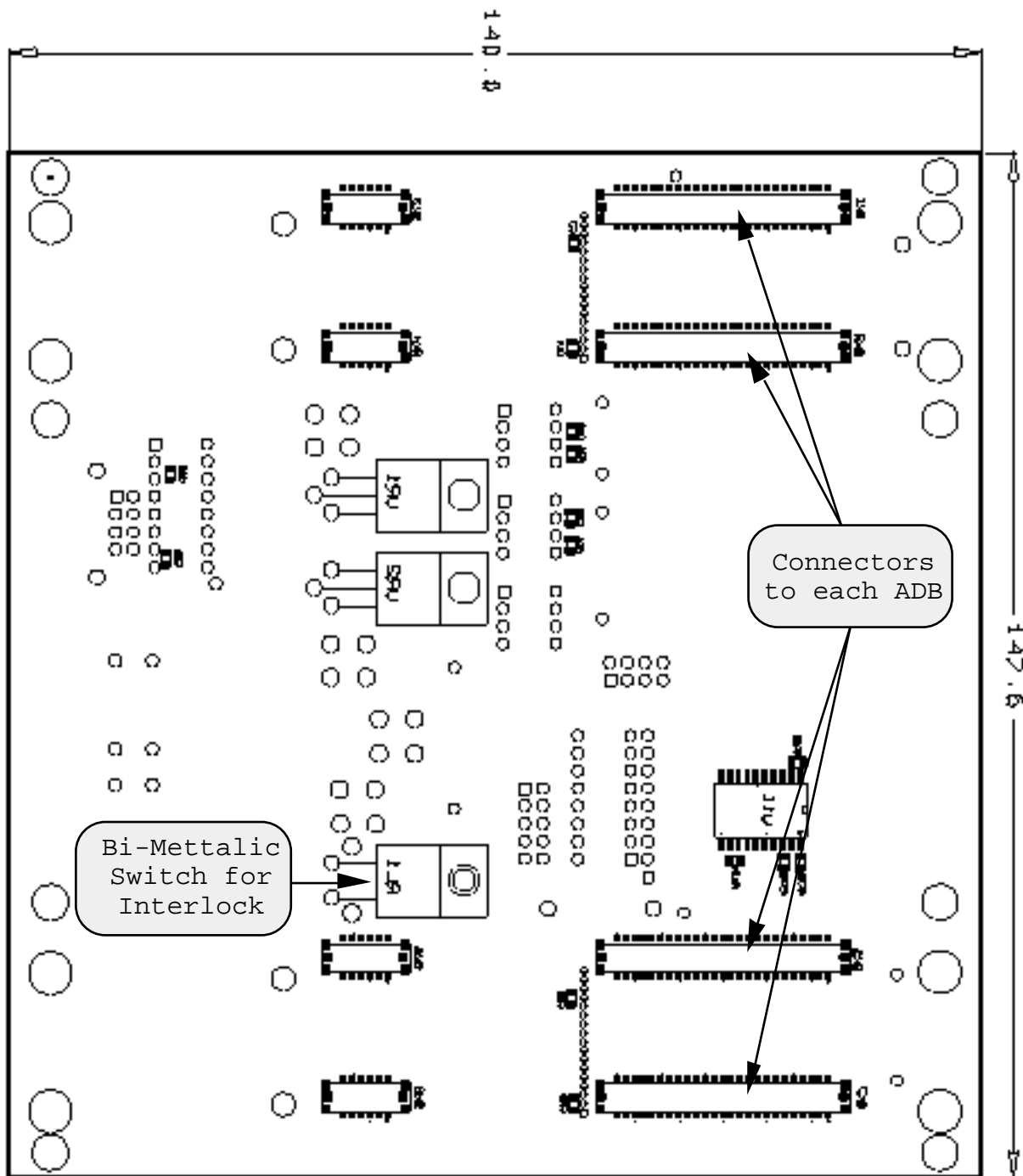


Figure 13 — Bottom side of the End-Cap I/O Board

The bottom component layout of the end-cap I/O board is shown in Figure 13. Note the connectors on the underside for the ADBs to plug into.

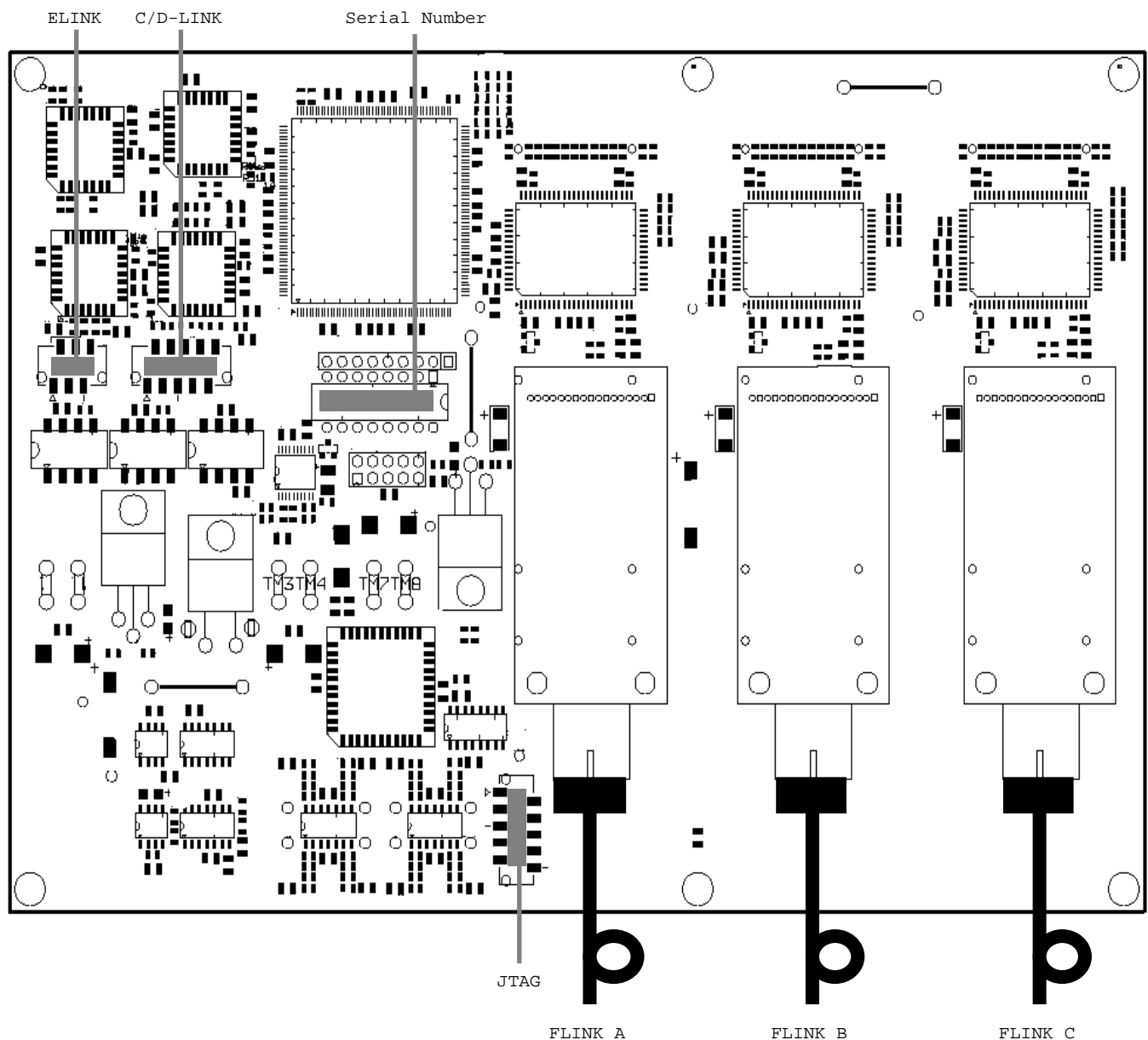


Figure 14 — B-IOB preliminary layout

A very preliminary layout of the components on the barrel IOB (B-IOB) is shown in Figure 14 (note the different orientation). To make this drawing two new ADBs have been added and the pitch between ADBs reduced. The control circuitry has been moved out radially, but no new chips are needed.

The size shown (13cm circumferentially by 16cm radially) is that currently allowed by the mechanical designers.