

BaBar Calorimeter DAQ ADC Board Description

Version Control:	
	Uncontrolled copy. This means that this copy of the document may not be the latest version. You can download the latest version via the WWW from the BaBar Home Page-> Electronics->Calorimeter->System and Board Descriptions.
	Controlled copy issued to:

Author:	john.dowdell@rl.ac.uk		
File Name:	JohnD HD:BaBar:Write-Ups:ADB Description:ADB Description		
First Modified:	14-Apr-96	Last Modified:	19-May-97

1. INTRODUCTION

This document describes the ADC board (ADB) of the BaBar Electromagnetic Calorimeter (EMC) Data AcQuisition (DAQ) system. This module will be used in both the barrel and end-cap of the detector.

This module processes the data from 12 crystals.

CONTENTS

1. INTRODUCTION.....	2
2. REVISION HISTORY.....	3
3. CARE CHIPS	4
3.1 BIAS VOLTAGES	5
3.2 CLOCKS.....	5
3.3 ELECTRONICS CONTROL REGISTER.....	5
3.4 INTERFACE TO THE PRE-AMPS	6
3.5 DISTRIBUTION OF THE PHOTODIODE BIAS VOLTAGE.....	6
4. DIGITISATION	6
4.1 ADC CLOCK.....	6
4.2 ADC REFERENCE VOLTAGES	6
4.3 ADC OUTPUT	6
5. DATA FORMATTING.....	7
6. CALIBRATION SIGNAL GENERATION.....	8
7. POWER DISTRIBUTION.....	9
8. ENVIRONMENTAL MONITORING FUNCTIONS.....	10
9. PIN-OUT OF CONNECTORS.....	12
10. PHYSICAL LAYOUT	15

3. CARE CHIPS

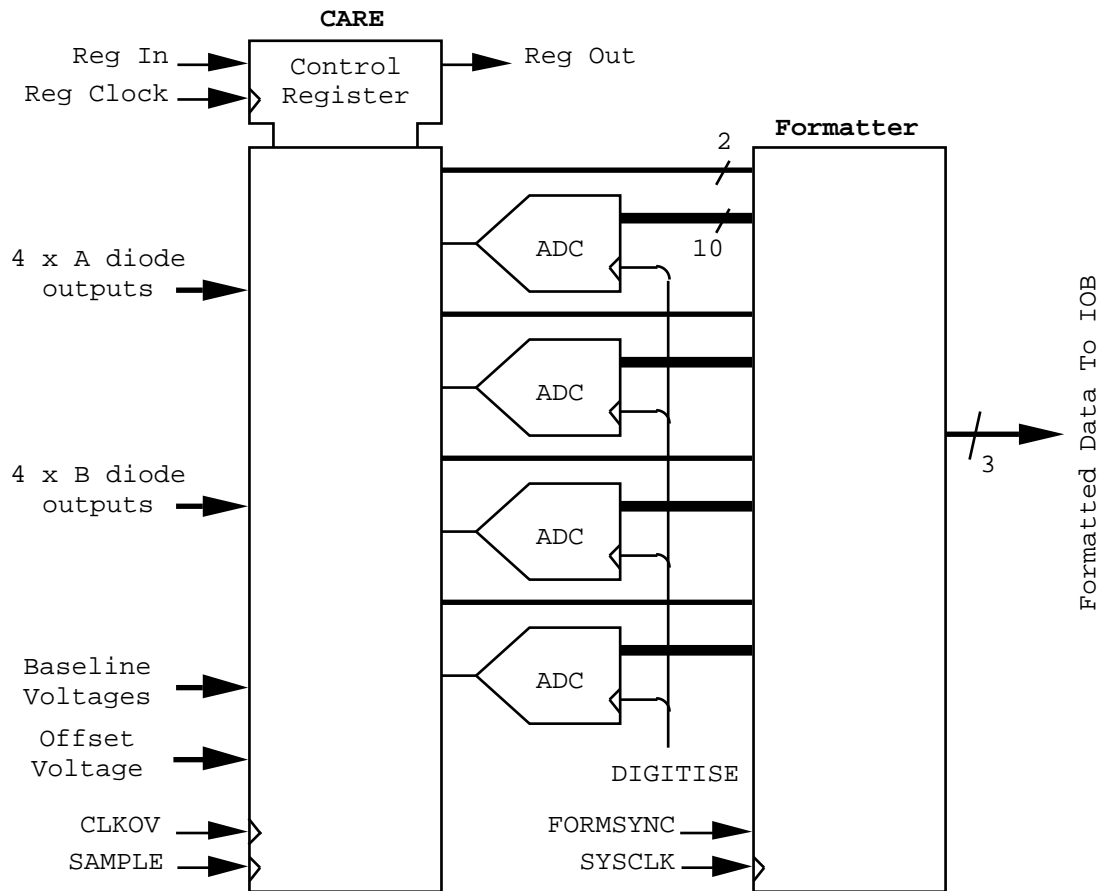


Figure 1 — Block Diagram of the Digitisation Logic

Figure 1 is a block diagram of the logic associated with one CARE chip (there are three such chips on the board for a total of twelve channels).

3.1 Bias Voltages

The various bias voltages required by the CAREs are handled in the following way:

Signal	Description	How treated
B1, B8	bias voltages	100nF decoupling to GND
Voutbaseline	1.3V bias voltage	100nF decoupling to GND
Vbaseline	DC bias for input stages	driven with 1.2V through an op-amp
Vobase	DC bias for output stages	connected to Vbaseline
Vcmpbias	bias current for comparator	30k resistor to +5V
Vcomp	threshold for saturation comparator	driven with 2.9V through an op-amp
Voffset	offset added by output stages	driven from a resistive divider via an op-amp

Therefore the Voutbaseline output, intended to drive the Vbaseline and Vobase inputs, is not yet used. This signal could be used instead of the external voltage from an op-amp if tests prove this mode of operation is successful and the variation of the voltage on this output from chip to chip is low enough that Vcomp does not have to be adjusted individually. The voltages are derived by dividing the output of a voltage reference using precision resistors.

Voffset can be adjusted by changing a resistive divider connected to a reference voltage.

3.2 Clocks

The clk_{sample} and clk_{cmp} clock inputs are connected to the SAMPLE clock from the I/O board, clk_{ov} is connected to CLKOV from the I/O board. These clocks run at 3.7MHz, the difference between them is described in the “EUROCARE 1 Description”.

3.3 Electronics Control Register

The CARE chips contain a six bit control register for each crystal. This is accessed as a simple shift register (the interface consists of data in, data out, data clock), bit zero is shifted in first.

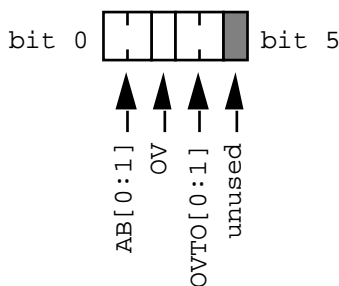


Figure 2 — CARE control register (per crystal)

The registers for all crystals on the ADC board are connected in series. The control bits for crystal one are shifted in first, then two, etc. up to twelve.

3.4 Interface to the Pre-amps

The connector between the fanout and ADC boards is a 2mm pitch, 5 row backplane style connector. The total number of pins is 250. This connector has an EMI shield around both mating halves. This shield is connected to the outer shield of the detector.

The eight inputs per pre-amp (two differential gain ranges) are connected directly to the connector from the fanout board. It is assumed that the AC coupling between the pre-amp and CARE chips is on the pre-amp board.

3.5 Distribution of the Photodiode Bias Voltage

The photodiode bias voltage is connected to the EFOB or bulkhead. From there it comes onto the ADB and is connected to one pin on the connector per pre-amp. This means that if a pre-amp develops a fault it is possible to isolate it by removing a pin.

4. DIGITISATION

The CARE output is connected directly to the input of the ADC.

4.1 ADC Clock

The ADC digitisation clock is connected to the `DIGITISE` clock from the I/O board. The frequency of this clock is programmable on the I/O board to be either 3.7MHz or 14.9MHz.

4.2 ADC Reference Voltages

The reference inputs are connected to the following voltages, derived by dividing the output of a voltage reference using precision resistors:

Top Reference	3.8V
Bottom Reference	1.6V

The voltage range of the output of the CARE (biased with the voltages shown in section 3.1) is nominally from 3.6V to 1.6V. Increasing the top reference to 3.8V allows for some threshold shift in the CARE. By increasing the voltage applied to the offset pin of the CARE, the baseline of the output can be decreased. The baseline will be set significantly less than 3.8V to allow the overshoot due to large AC coupled signals to be digitised.

The ADC is a ten bit device, so a least significant bit corresponds to 2.2mV.

4.3 ADC Output

The outputs of the ADC are updated on the falling edge of the digitisation clock (this is a feature of the device intended to reduce interference from transitions of the output to the input).

The latency of the ADC is four digitisation clocks. This means that the output of the ADC corresponds to the input voltage four digitisation clock periods ago.

5. DATA FORMATTING

The data formatter is clocked by `SYSCLK` from the I/O board (59.5MHz). This corresponds to the frequency with which data must be presented to the G-LINK at the output of the formatter. The `FORMSYNC` input from the protocol receiver on the I/O board is used to signal to the formatter when new data is available from the CARE and ADCs.

The range outputs from a CARE and the output of the corresponding four ADCs (a total of 48 bits) are latched into the formatter on the rising edge of `SYSCLK` just before the rising edge of `SAMPLE` (coincident with a '1' on `FORMSYNC`). Thereafter they are shifted out nine bits at a time, using `SYSCLK`, directly to the connector to the I/O board.

If the `DIGITISE` clock runs at 3.7MHz then the ADC values into the formatter will be four `SAMPLE` clock periods behind the range bits from the CAREs. If the `DIGITISE` clock is 14.9MHz then three out of every four digitisations will be discarded automatically and the range bits and ADC sample will be in alignment. The formatter will automatically compensate for this latency shift on the ADC board.

The formatter is followed by an TTL to ECL converter. These chips drive the connector to the I/O board with ECL signals.

As a test feature, the `LINKTEST` signal from the IOB (when logic high) causes the data formatters to produce a known, repeating pattern: the three bits from each formatter behave like a three bit counter. The counter is reset to zero using `FORMSYNC`, so the synchronisation of the formatters to this signal is also tested.

6. CALIBRATION SIGNAL GENERATION

The pre-amps require calibration signals of the following format:

- a CMOS capacitor select, and
- a combined calibration voltage and strobe as shown below.

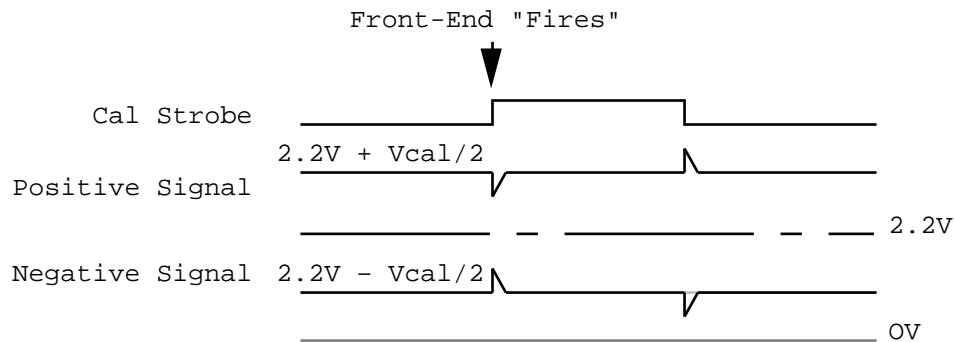


Figure 3 — The combined calibration strobe and voltage

The IOB supplies two independent capacitor selects. These are buffered on the ADB and sent to all A and all B diodes respectively.

The IOB also supplies four independent combined voltage and strobes. These are buffered with unity gain buffers on the ADB and connected to:

- diode A of all odd numbered crystals, or
- diode B of all odd numbered crystals, or
- diode A of all even numbered crystals, or
- diode B of all even numbered crystals

7. POWER DISTRIBUTION

The power supplies used or passed through the ADC board are shown below.

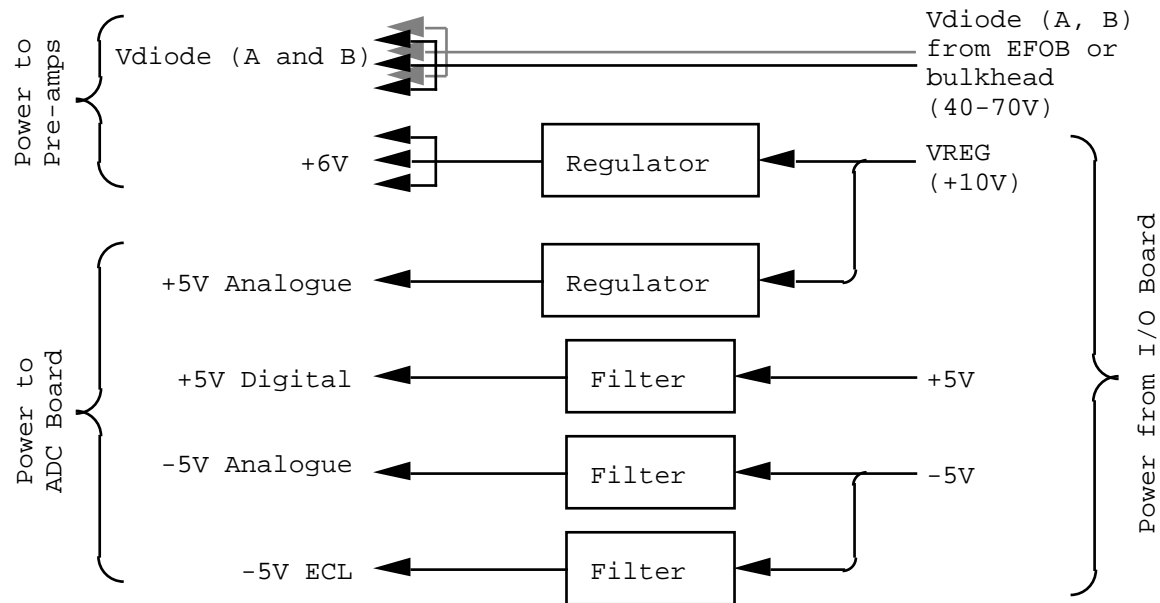


Figure 4 — ADC Board Power Supplies

The four voltages on the right hand side come from the power supply units via the I/O board. They are then processed as shown below:

- Power for the A photodiodes (V_{diodeA}) is fanned out from an input from the EFOB or bulkhead. Likewise power for the B photodiodes (V_{diodeB}) is fanned out from an input from the EFOB or bulkhead
- Power for the pre-amps (+6V) is derived via a regulator from the VREG (+10V).
- +5V analogue is derived from a regulator.
- +5V digital is simply filtered.
- -5V ECL (for the TTL to ECL converters) is simply filtered.
- -5V analogue (for the rest of the analogue circuitry) is simply filtered.

The reason +5V digital is not regulated from VREG is simply that the current drawn is too high. Regulating this on-detector would generate too much heat. The analogue power supplies are regulated because they are sensitive, and the current drawn is small enough that the heat generated is acceptable.

The total power consumption per supply for an ADB is approximately:

+9V	1 A
+5V	1 A
-5V	1 A

The total power dissipated on the ADC board is of the order of 19W.

There will be electrostatic shielding enclosures over the top and bottom of the board and between the CAREs and formatters. This shielding will be connected to the outer shield of the detector.

The hot components will be in thermal contact with the screen cans, so cooling will be performed by connecting the shields to a cooled surface.

8. ENVIRONMENTAL MONITORING FUNCTIONS

Full details of the environmental monitoring functions provided by the ADC and I/O boards can be found in the I/O board description. This section deals only with what is on the ADB.

The output of the +6V and +5V CARE voltage regulators are monitored by the environmental monitoring system. These voltages must be monitored on the ADC board because they cannot be observed anywhere else, and they are critical to the operation of the electronics. In addition, if there is little overhead, the control voltages for the CAREs and ADCs could be monitored.

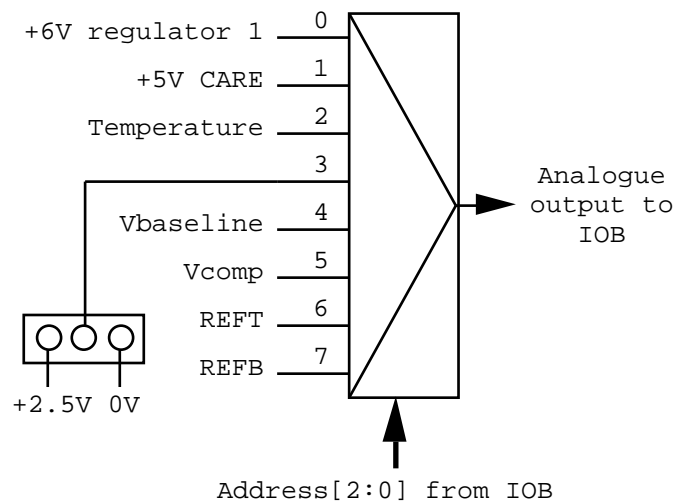


Figure 5 — Environmental monitoring multiplexer on ADB

The ADC board contains an eight-to-one analogue multiplexer to select among the possible quantities to be measured, see Figure 5. Input number three is in principle unused, so as a test feature on the prototype it can be tied to 0V, +2.5V or left open.

The interface between ADB and IOB is therefore three bits of digital information from the IOB to select which quantity to pass through to the analogue output and back to the IOB.

The ADC on the IOB can only handle voltages up to 4V, so some of these quantities have scaling factors applied before the multiplexer. The quantities that can be measured and the approximate scaling factors used are shown in the following table:

MUX address	Description	Expected Voltage	Scale Factor
0	+6V regulator 1	6	2
1	+5V regulator for CARE	5	2
2	Temperature	10 mV/°K	1
3	Jumper selectable (0V/2.5V/open)	—	1
4	v _{baseline} for CAREs	1.2	1
5	v _{comp} for CAREs	2.9	1
6	ADC top reference voltage (REF _T)	3.8	2
7	ADC bottom reference voltage (REF _B)	1.6	1

9. PIN-OUT OF CONNECTORS

The connector to the fanout board is a 2mm pitch, 5 row, backplane style connector.

Column	Row A	Row B	Row C	Row D	Row E
1	—	—	—	—	—
2	1A x 32	1A x 32 *	1A +6V	1B x 32	1B x 32 *
3	1A VDIODE	1A CALSEL	GND	1B VDIODE	1B CALSEL
4	1A x 1 *	1A x 1	1B +6V	1B x 1	1B x 1 *
5	1A VCALP	1A VCALM	GND	1B VCALM	1B VCALP
6	2A x 32	2A x 32 *	2A +6V	2B x 32	2B x 32 *
7	2A VDIODE	2A CALSEL	GND	2B VDIODE	2B CALSEL
8	2A x 1 *	2A x 1	2B +6V	2B x 1	2B x 1 *
9	2A VCALP	2A VCALM	GND	2B VCALM	2B VCALP
10	3A x 32	3A x 32 *	3A +6V	3B x 32	3B x 32 *
11	3A VDIODE	3A CALSEL	GND	3B VDIODE	3B CALSEL
12	3A x 1 *	3A x 1	3B +6V	3B x 1	3B x 1 *
13	3A VCALP	3A VCALM	GND	3B VCALM	3B VCALP
14	4A x 32	4A x 32 *	4A +6V	4B x 32	4B x 32 *
15	4A VDIODE	4A CALSEL	GND	4B VDIODE	4B CALSEL
16	4A x 1 *	4A x 1	4B +6V	4B x 1	4B x 1 *
17	4A VCALP	4A VCALM	GND	4B VCALM	4B VCALP
18	5A x 32	5A x 32 *	5A +6V	5B x 32	5B x 32 *
19	5A VDIODE	5A CALSEL	GND	5B VDIODE	5B CALSEL
20	5A x 1 *	5A x 1	5B +6V	5B x 1	5B x 1 *
21	5A VCALP	5A VCALM	GND	5B VCALM	5B VCALP
22	6A x 32	6A x 32 *	6A +6V	6B x 32	6B x 32 *
23	6A VDIODE	6A CALSEL	GND	6B VDIODE	6B CALSEL
24	6A x 1 *	6A x 1	6B +6V	6B x 1	6B x 1 *
25	6A VCALP	6A VCALM	GND	6B VCALM	6B VCALP
26	7A x 32	7A x 32 *	7A +6V	7B x 32	7B x 32 *
27	7A VDIODE	7A CALSEL	GND	7B VDIODE	7B CALSEL
28	7A x 1 *	7A x 1	7B +6V	7B x 1	7B x 1 *
29	7A VCALP	7A VCALM	GND	7B VCALM	7B VCALP
30	8A x 32	8A x 32 *	8A +6V	8B x 32	8B x 32 *
31	8A VDIODE	8A CALSEL	GND	8B VDIODE	8B CALSEL
32	8A x 1 *	8A x 1	8B +6V	8B x 1	8B x 1 *
33	8A VCALP	8A VCALM	GND	8B VCALM	8B VCALP
34	9A x 32	9A x 32 *	9A +6V	9B x 32	9B x 32 *
35	9A VDIODE	9A CALSEL	GND	9B VDIODE	9B CALSEL
36	9A x 1 *	9A x 1	9B +6V	9B x 1	9B x 1 *
37	9A VCALP	9A VCALM	GND	9B VCALM	9B VCALP
38	10A x 32	10A x 32 *	10A +6V	10B x 32	10B x 32 *
39	10A VDIODE	10A CALSEL	GND	10B VDIODE	10B CALSEL
40	10A x 1 *	10A x 1	10B +6V	10B x 1	10B x 1 *
41	10A VCALP	10A VCALM	GND	10B VCALM	10B VCALP
42	11A x 32	11A x 32 *	11A +6V	11B x 32	11B x 32 *
43	11A VDIODE	11A CALSEL	GND	11B VDIODE	11B CALSEL
44	11A x 1 *	11A x 1	11B +6V	11B x 1	11B x 1 *

Column	Row A	Row B	Row C	Row D	Row E
45	11A VCALP	11A VCALM	GND	11B VCALM	11B VCALP
46	12A x 32	12A x 32 *	12A +6V	12B x 32	12B x 32 *
47	12A VDIODE	12A CALSEL	GND	12B VDIODE	12B CALSEL
48	12A x 1 *	12A x 1	12B +6V	12B x 1	12B x 1 *
49	12A VCALP	12A VCALM	GND	12B VCALM	12B VCALP
50	—	VDIODE for A diodes	—	VDIODE for B diodes	—

There are two connectors to the I/O board: a 50 way and a 12 way surface mount connector.

Signal	Pin	Pin	Signal
VCALP (0)	1	2	VCALM (0)
VCALP (1)	3	4	VCALM (1)
VCALP (2)	5	6	VCALM (2)
GND	7	8	GND
VCALP (3)	9	10	VCALM (3)
CALSEL (0)	11	12	CALSEL (1)

Signal	Pin	Pin	Signal
Clean shield ground	1	2	GND
LINKTEST	3	4	DCLKSEL
Clock for CARE control register	5	6	GND
GND	7	8	CARE control register data from IOB
CARE control register data to IOB	9	10	GND
GND	11	12	SAMPLE
DIGITISE	13	14	GND
GND	15	16	SYSCLK
FORMSYNC	17	18	GND
GND	19	20	CLKOV
Formatter data bit 0 (ECL)	21	22	GND
GND	23	24	Formatter data bit 1 (ECL)
Formatter data bit 2 (ECL)	25	26	GND
GND	27	28	Formatter data bit 3 (ECL)
Formatter data bit 4 (ECL)	29	30	GND
GND	31	32	Formatter data bit 5 (ECL)
Formatter data bit 6 (ECL)	33	34	GND
GND	35	36	Formatter data bit 7 (ECL)
Formatter data bit 8 (ECL)	37	38	GND
Monitoring MUX address A0	39	40	Monitoring MUX address A1
Monitoring MUX address A2	41	42	Monitoring MUX analogue output
VREG power supply	43	44	GND
+5V power supply	45	46	GND
+5V power supply	47	48	GND
-5V power supply	49	50	GND

10. PHYSICAL LAYOUT

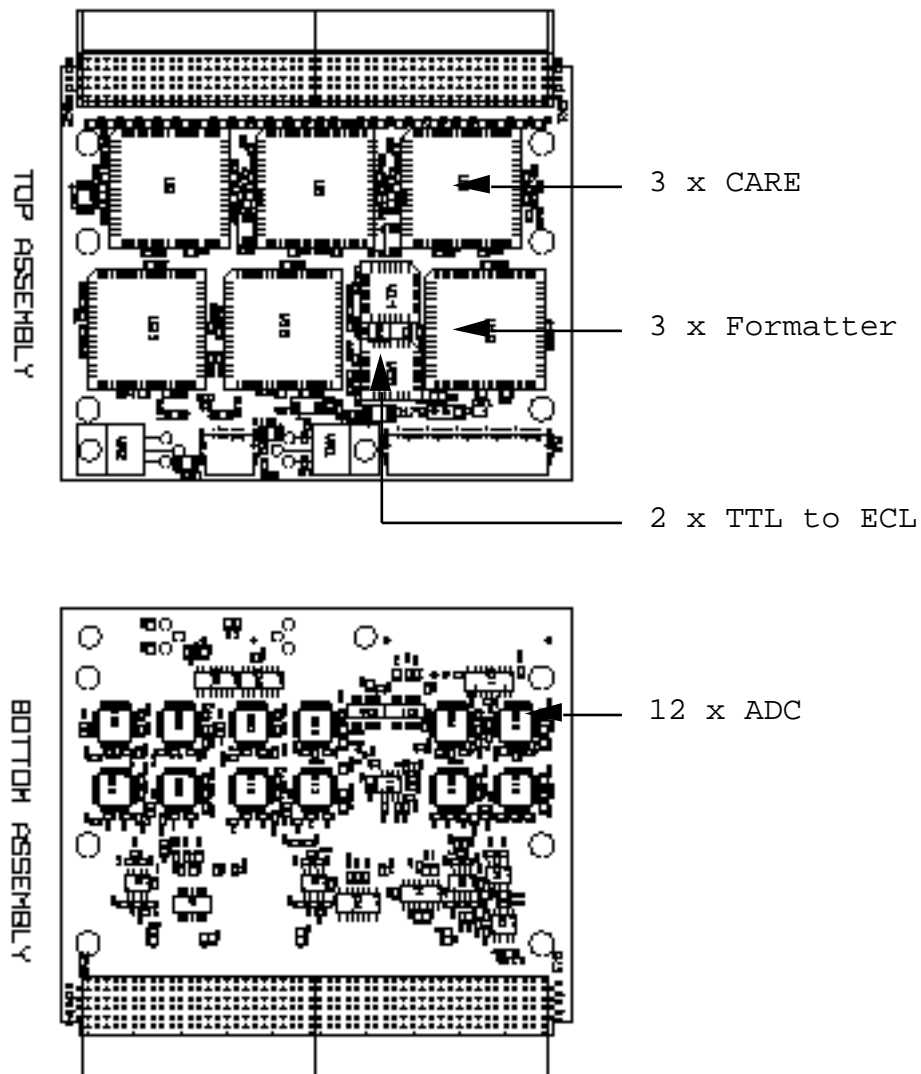


Figure 6 — ADB preliminary layout

The layout of the board is shown in Figure 6.