

# BaBar Calorimeter DAQ/Trigger RAL2302 Driver/Receiver Module (G-LINK & Finisar Daughterboard)

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## 1. THE OPTICAL TRANSCEIVER DAUGHTERBOARD

The transmitter section consists of a G-LINK transmitter (HDMP-1012) and Finisar transmitter (FTM-8510-1-0)<sup>1</sup>. The receiver section consists of a Finisar receiver (FRM-8510-1) and G-LINK receiver (HDMP-1014). All data outputs and most controls are brought out on pins to the motherboard, including the pins to access the Finisar built in Test/Diagnostics Port<sup>2</sup>.

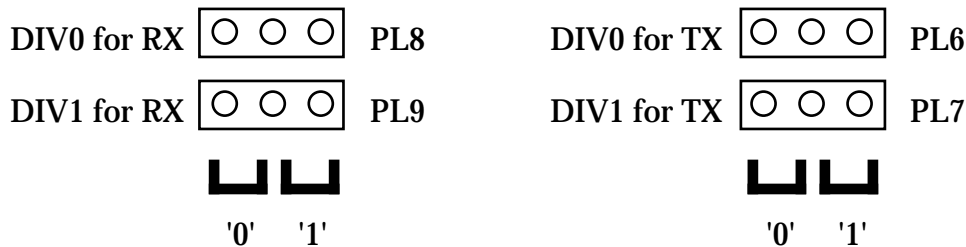


Figure 1 — Setting DIV0/1

The clock divider DIV0, DIV1 for the TX and RX and selection between simplex and duplex operation are set by links on the daughterboard. See Figure 1 for the jumper positions.

In duplex mode only, it is possible to operate the transmitting and receiving G-LINKs in loop-back mode, under the control of bits in a register. In this mode data flows not down the fibre and back, but directly from the transmitter to receiver using the alternate inputs and outputs provided for this purpose. This is used as a test facility.

<sup>1</sup> “Application Note: Interfacing Various Gb/s Chip Sets to FTR-XX10, FTM-XX10 and FRM-XX10”; Finisar AN-2012; July 1994

<sup>2</sup> “Application Note: Using the Built-in Test/Diagnostics Port on FTR-XX10, FTM-XX10 and FRM-XX10”; Finisar AN-2010; February 1994

## 2. THE DRIVER/RECEIVER MOTHERBOARD

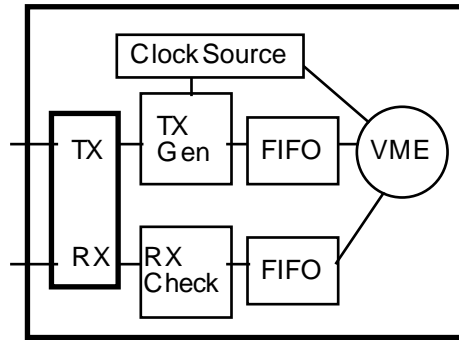


Figure 2 — Block diagram of RAL2301

The block diagram of this board is shown in Figure 2.

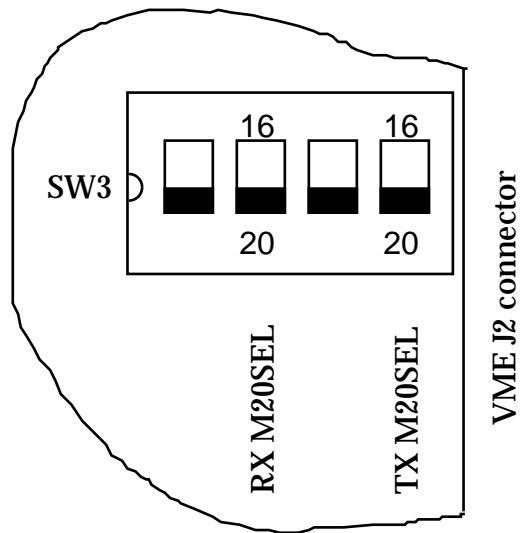


Figure 3 — Flag and data set-up

Control of the width of the transmitted and received words (16 or 20 bit) is performed by a DIP switch on the daughterboard (marked SW3), see Figure 3.

### 2.1 Transmitter

In order to be as flexible as possible the data to be sent is stored in a FIFO via the VME interface. When the software has filled the FIFO the transmitter is told to send the contents of the FIFO down the link. There are two possibilities at this point:

- the contents of the FIFO are sent and the link returns to idle, or
- the data read from the FIFO is written back in and hence the contents of the FIFO are sent indefinitely. The transmitter must be told to stop sending data. Selection of this mode is performed by setting the AUTOWRITE bit in the module mode register.

In some applications it is desired to send zero data when idle instead of nothing. This is supported by setting the ALLSEND bit in a register.

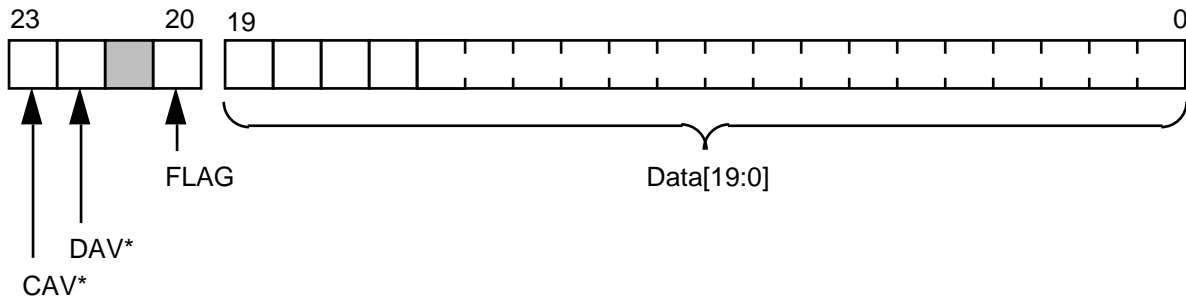


Figure 4 — Transmitted data format in FIFO

The word in the FIFO determines whether a control or data word is sent etc., as shown in Figure 4.

It is possible to get the transmitter to generate a pseudo-random sequence to test the link by setting the LFSREN bit in the module mode register.

## 2.2 Monitoring the Laser Transmitter

The Finisar transmitter diagnostic port is accessible by a VME master.

## 2.3 Receiver

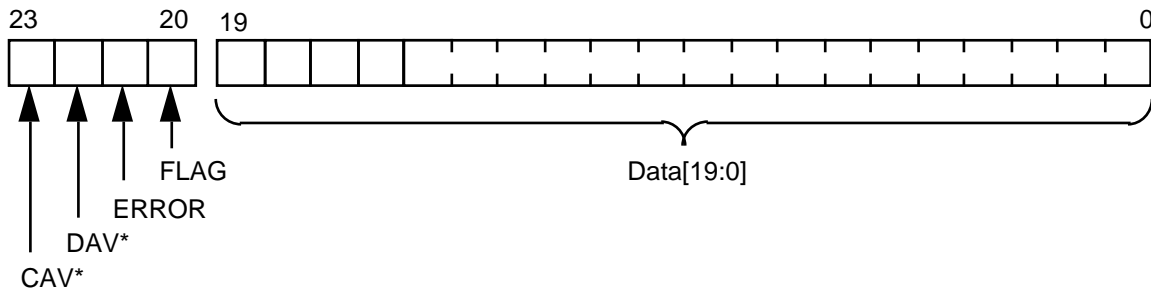


Figure 5 — Received data format

Received data is written into a FIFO. The format is shown in Figure 5.

## 2.4 Writing data into the RX FIFO

The module can either be idle or armed to record data. In the idle state it never records data. In the armed state it records data in the FIFO when any of the following signals is active: CAV\*, DAV\* or ERROR.

The FIFO has a fixed depth (varying from 512 to 4096 words, depending on the actual chip installed) and when it fills up it stops recording data. The FIFO can be operated as a circular buffer by reading from it at the same rate as it is written when the FIFO becomes almost full (i.e. only seven free entries). Selection between these two modes is performed using the Autoread (AR) bit in the mode register.

The following events will make the module move from the idle to the armed state:

- The assertion of the RUN front-panel NIM input (if it is enabled in the mode register), or
- The assertion of the SW\_RUN bit in the mode register by software.

The following events will make the module move from the armed back to the idle state:

- The de-assertion of the RUN front-panel NIM input (or the de-assertion of its enable bit in the mode register),
- The de-assertion of the SW\_RUN bit in the mode register by software,
- The assertion of the ERROR signal by the G-LINK receiver (if enabled in the mode register), or

- The occurrence of a pseudo-random sequence error (if enabled in the mode register).

The ability to mask off some of these transitions is provided for flexibility.

## 2.5 Acquiring Pseudo-Random Data

Testing of the link for loss of synchronisation and bit error rate is best done automatically with pseudo-random data. If the bit error rate is  $10E-14$  we expect one error every 20 hours at a word rate (20 bit words) of 59.5MHz.

In this mode the formatter on the ADC board produces a stream of data from a linear feedback shift register (LFSR) — formatting into packets is dropped. In order to make the test deterministic:

- 1) the TX is made idle (neither CAV\* nor DAV\* sent)
- 2) the LFSR is set to 0x00001 (the seed)
- 3) the TX is told to go. It now asserts DAV\* only and sends the sequence.

The transmitter and receiver logic automatically knows from the setting of the switches in Figure 3 whether to generate (or check) a sixteen or twenty bit pseudo-random pattern.

A maximal length 20 bit LFSR can be implemented using a shift register (Q[19:0], data enters through Q[0]) where Q[0] is generated from the XOR of data bits Q[19] and Q[16]. Note that the initial state of the shift register must not be 0x00000! (Think about it...)

For a maximal length 16 bit LFSR, Q[0] is generated from Q[3] xor Q[12] xor Q[14] xor Q[15].

The receiver starts with the same initial value and should generate the same sequence as that received from the transmitter. If a received word and a local word are different there has been a bit error. In order to monitor this process, the number of words received by the de-formatter is scaled in a 48 bit counter and the number of errors is scaled by a 16 bit counter. The scalars only increment when the module is recording data. Note also that the scalars stop scaling while being read over VME; so don't read then too often or you will prolong the test!

During this process the FIFO records the data from the link and the detection of an error in the sequence can be used to stop recording data. The value that caused the error and a history beforehand is now stored in the FIFO for checking.

## 2.6 Acquiring Test Beam Data

The front-panel NIM input can be used to start data acquisition and stop it after a 'trigger'.

## 2.7 Emulating the Transition Board Interface

The bits in the FIFOs referred to as FLAG bits are now used to emulate the transition board. This interface consists of clock and data in PECL signal standard out of the module and clock and data also in PECL into the module. The clock is the same clock used to drive the GLINK.

Because the return data has to be clocked into the RX FIFO using the clock recovered from the GLINK a variable delay (changed using handbags) is provided on the daughterboard to align the data properly with the clock.

## 2.8 Emulating the ELINK Interface

The ELINK interface consists of a clock and data out of the 2302 and a data bit returning. These signals are driven directly from bits in registers. Due to unforeseen circumstances the 20mA current loop drivers could not be incorporated onto this module, so the I/O is at TTL levels.

### 2.9 Register Map

The following registers are accessible from the VME (the module is configured as an A24 D16 slave only — only 24 bit address, 16 bit data accesses are supported):

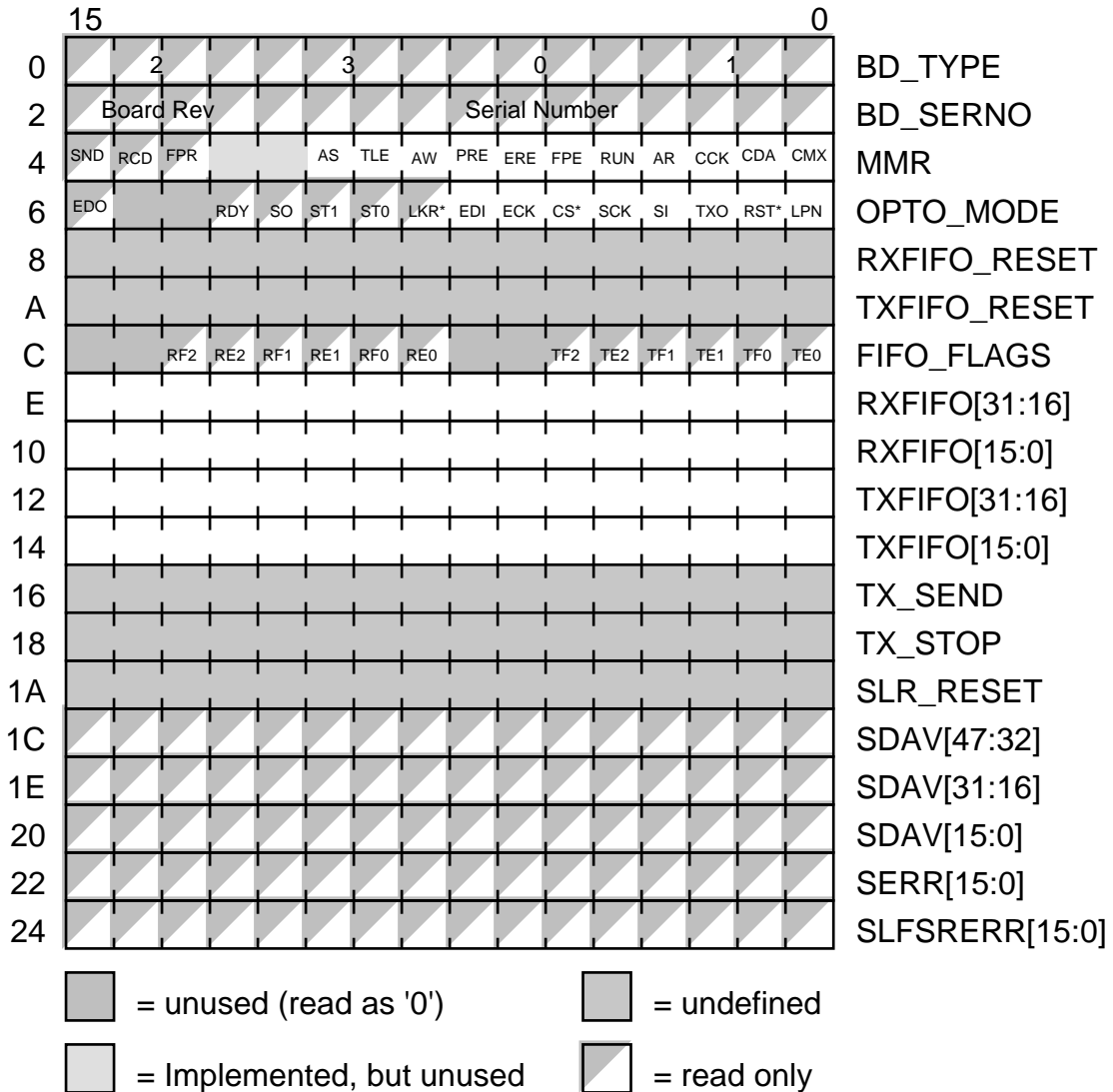


Figure 6 — RAL2301 Register Map

The meaning of the bits will be discussed in the following sections.

#### 2.9.1 Board Type (BD\_TYPE)

Reading from this register return the board type number (0x2301 for RAL2301).

#### 2.9.2 Board Serial Number (BD\_SERNO)

Reading from this register returns the board revision and serial numbers. The revision number should be 0x1. The serial number is unique to each module, it starts at 0x001.

### 2.9.3 Module Mode Register (MMR)

This register is intended to hold set-ups that are global to the whole module.

SND (Sending) flags whether the transmitter is sending data or not. If it is sending data the VME will not be able to access the FIFO.

- 0 Transmitter is idle
- 1 Transmitter is sending from the FIFO

RCD (Record) flags whether the module is in record mode or idle.

- 0 module is idle — no data recording
- 1 module is in record mode.

FPR (Front Panel Run) flags the state of the NIM 'RUN' input on the front panel.

- 0 input is '0'
- 1 input is '1' (requesting run).

AS (Allways Send) specifies whether the transmit link can ever be 'idle' (neither DAV\* nor CAV\* asserted).

- 0 transmit link is idle if not sending from the FIFO
- 1 transmit link sends zero data words if not sending from the FIFO

TLE (TX LFSR Enable) specifies whether the transmitter sends a pseudo-random pattern instead of FIFO data.

- 0 send from FIFO
- 1 send a pseudo-random sequence.

AW (Auto-Write) controls whether the transmit FIFO is refreshed or not.

- 0 FIFO contents are sent once.
- 1 FIFO contents are refreshed (each value read is written back in) so the contents are sent indefinitely.

PRE (Pseudo-random Error Enable) allows the occurrence of a pseudo-random sequence error to bring the module out of record mode.

- 0 errors have no effect
- 1 an error will bring the module out of record mode.

ERE (Error Enable) allows the occurrence of an error from the G-LINK to bring the module out of record mode.

- 0 errors have no effect
- 1 an error will bring the module out of record mode.

FPE (Front Panel Enable) enables the front panel run signal.

- 0 front panel run signal has no effect
- 1 module will go into/out of record mode as requested by the front panel run signal.

RUN (software run signal) asserting this signal will put the module into record mode.

- 0 no control action
- 1 module is put into run mode

AR (auto-read) controls whether the FIFO is used as a circular buffer or not.

- 0 FIFO fills up and stops
- 1 automatically read from FIFO when almost full to form a circular buffer

The next three bits are used to program the ICD2051 clock generator. Refer to the data sheet for more information:

CCK is the clock to clock the serial data into the internal control register (active rising edge).

CDA is the serial data to clock into the internal control register

CMX determines whether the PLL is enabled or not.

- 0 PLL is disabled
- 1 PLL is enabled

#### 2.9.4 Optical Link Mode Register

RDY is a ready signal indicating the Finisar transmitter is ready for access to the test/diagnostic port.

SO is bit serial output data from the Finisar transmitter

ST[1:0] is the state of the state register used for the link start-up state machine.

LKR\* (LINKRDY\*) Active low, indicates that the link is ready to receive data.

CS\* (chip select, active low) selects the Finisar test/diagnostic port.

SCK is a serial shift clock into the Finisar transmitter test/diagnostic port

SI is bit serial data into the Finisar transmitter test/diagnostic port

TXO (TX\_OFF) turns the Finisar transmitter on and off (polarity to be clarified).

RST\* (RESET\*) resets the link when asserted and initiates the start-up sequence when de-asserted.

- 0 Reset the transmitter
- 1 Start up the link then normal operation

LPN (LOOP ENABLE) controls whether serial data is sent to the ADC board or looped back to the local G-LINK receiver.

- 0 Data sent to/received from the ADC board
- 1 Data looped back

ECK is the ELINK clock

EDI is data from 2302 onto the ELINK

EDO is data from ELINK into the 2302

#### 2.9.4 RXFIFO Reset Register (RXFIFO\_RESET)

Accessing this register resets the receive FIFO. Instead of leaving the FIFO empty it actually leaves it with one word containing 0x00. This has to be discarded in software.

#### 2.9.6 TXFIFO Reset Register (TXFIFO\_RESET)

Accessing this register resets the transmit FIFO. Instead of leaving the FIFO empty it actually leaves it with one word containing 0x00. This has to be removed by software.

#### 2.9.7 FIFO Flag Register (FIFO\_FLAGS)

Reading from this register returns the value of the full and empty flags of the six 8-bit FIFOs. EF is empty flag (active high), FF is full flag (active high).

### 2.9.8 RXFIFO Data Register (RXFIFO[31:0])

Reading from this register removes the next value from the receive FIFO and returns it. Writing writes a value into the receive FIFO, iff there is a decent clock from the receiving G-LINK!

### 2.9.9 TXFIFO Data Register (TXFIFO[31:0])

Reading from this register removes the next value from the transmit FIFO and returns it. Writing writes a value into the transmit FIFO.

### 2.9.10 Transmit Send (TXSEND)

Accessing this register causes the contents of the transmit FIFO to be sent down the link.

### 2.9.11 Transmit Stop (TXSTOP)

Accessing this register causes the transmission of the contents of the transmit FIFO to be stopped.

### 2.9.12 Scaler Reset Register (SLR\_RESET)

Accessing this register clears the following scalers.

### 2.9.13 DAV\* Scaler (SDAV[47:0])

This scaler counts the number of clock cycles that DAV\* is asserted for, while the module is in record mode. The scaler stops counting while it is read over VME.

If the G-LINK clock is 59.5MHz this scaler can run for 54 days without overflowing.

### 2.9.14 ERROR Scaler (SERR[7:0])

This scaler counts the number of received data words that are flagged as errors by the G-LINK receiver, while the module is in record mode. The scaler stops counting while it is read over VME.

During link start-up this scaler is likely to count wildly. It should be reset after link start-up to give an accurate indication of link performance.

### 2.9.15 LFSR Sequence Error Scaler (SLFSRERR[7:0])

This scaler counts the number of received data words that do not follow the correct pseudo-random sequence, while the module is in record mode. The contents of the scaler are only valid if the transmitter is sending the pseudo-random sequence! The scaler stops counting while it is read over VME.