



---

# L1 Simulation Upgrade

July 12<sup>th</sup>, 2004  
Simulation Workshop

Eric Torrence  
University of Oregon

Apologies to L3 and EMT...



# Overview

---



L1 DCT simulation is being rewritten from scratch.

Why?

DCT Hardware Upgrade (PTD -> ZPD)

- New boards and algorithms
- Added flexibility needed (old/new hardware)
- Can not be accommodated with existing code

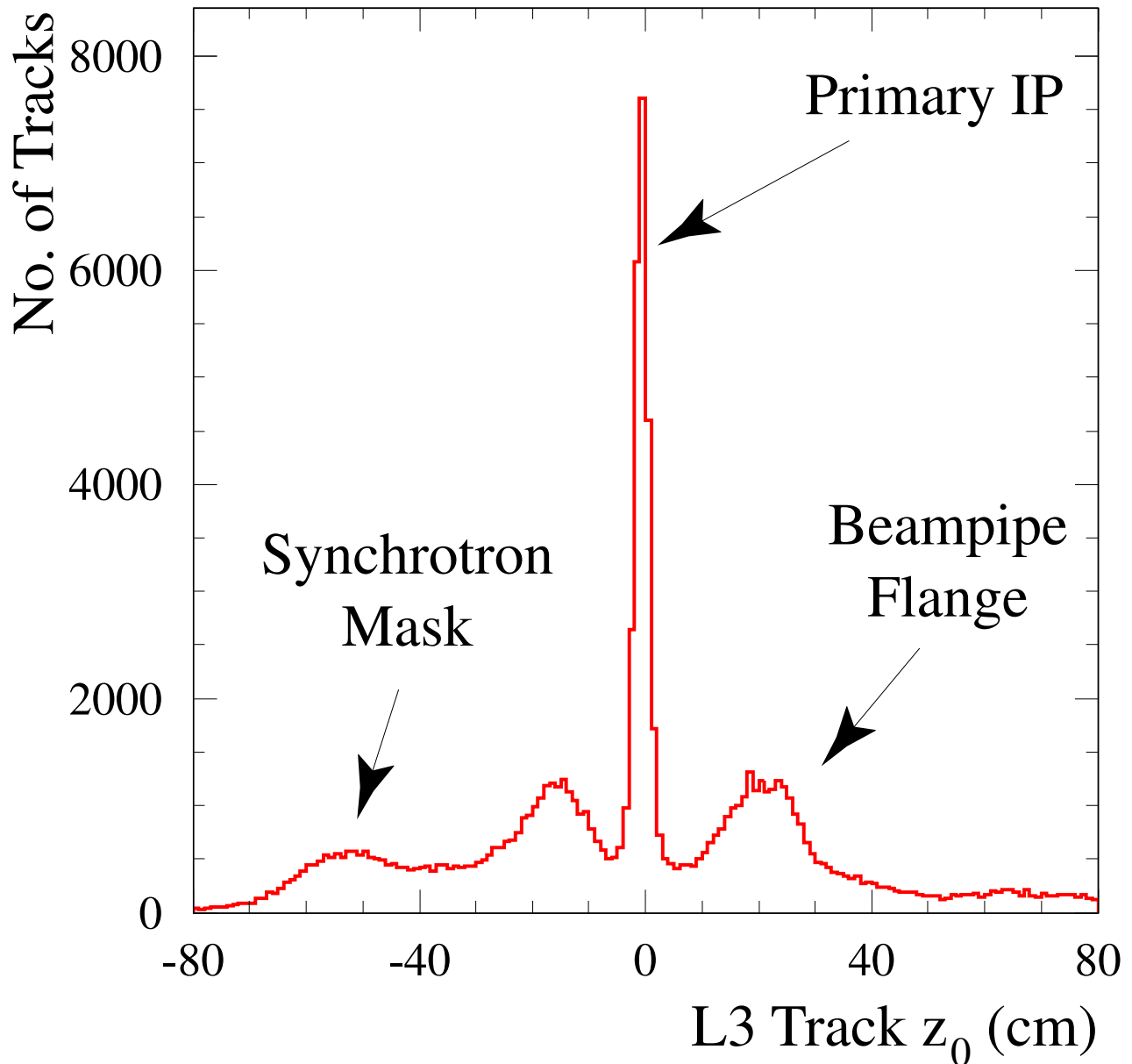
trgDC was a hack which was supposed to last for ~6 months. It is now 5 years later...

General Code Improvements

- Simulation configured just as hardware **configDB, no flat files/magic numbers**
- Better board-level validation
- Better (more transparent) design
- More flexibility for future



# Why Upgrade?

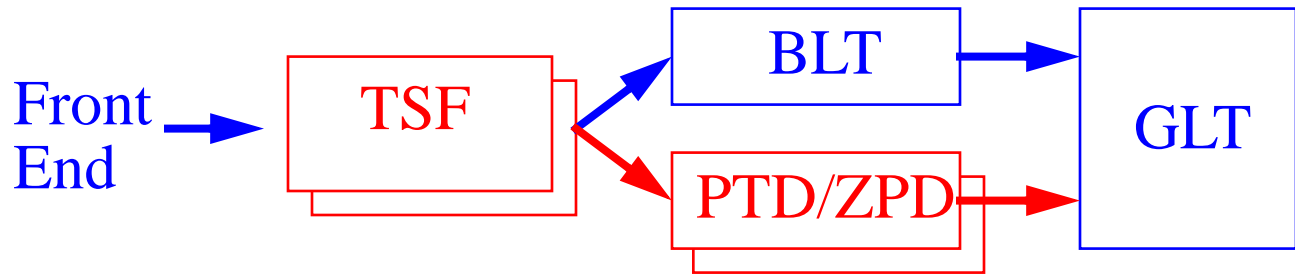


Many tracks at L1 are junk

Simple cut on  $z_0$  with  $\sigma_z \sim 1$  cm would help...

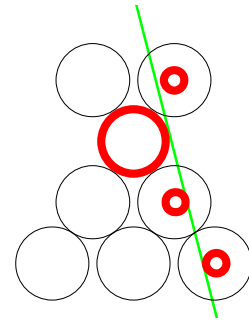


# Trigger Upgrade Overview



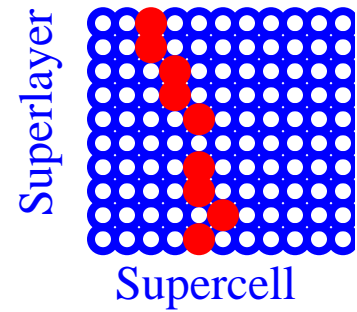
## Track Segment Finder (TSF)

24 TSF boards, all replaced



## Binary Link Tracker (BLT)

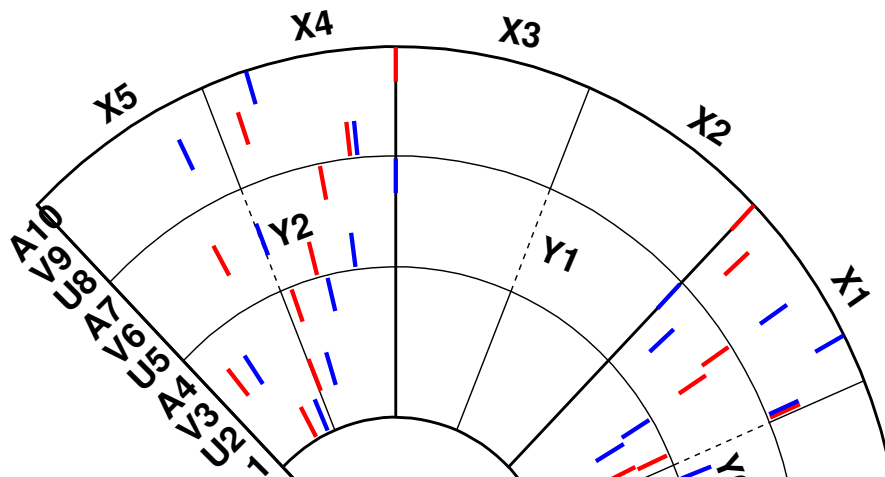
1 BLT board, unchanged



## $P_T$ Discriminator (PTD)

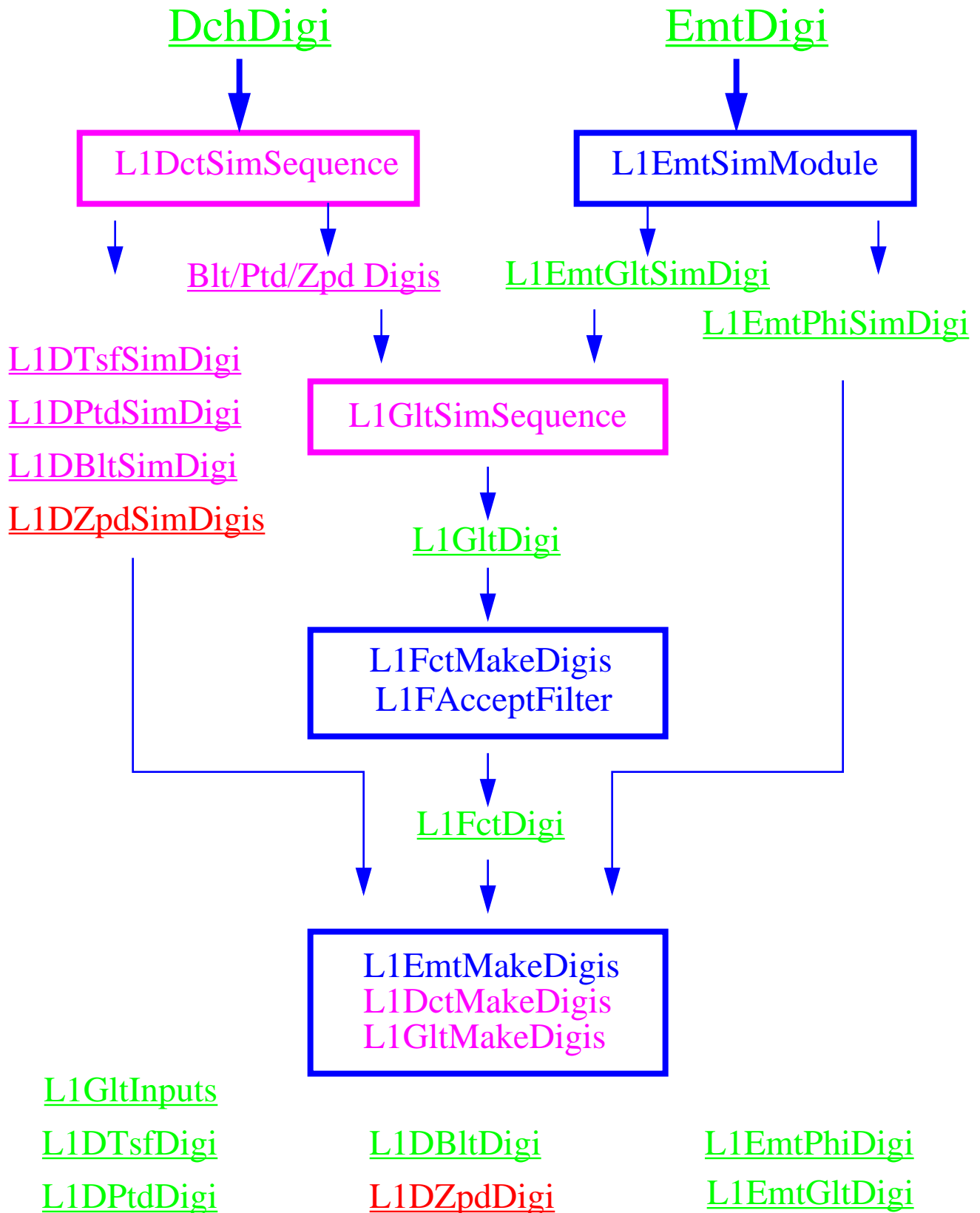
8 PTD Boards

replace with ZPD





# L1 Simulation Roadmap





# trgDC comparison

---



## Old trgDC event flow

```
loop over time ticks {
    doTSF()
    doPTD()
    doBLT()
    doGLT()
}
```

Data internally stored in **COMMON** arrays  
Clock conversions (clk4 - clk8) done “by hand”

## New L1Sim event flow

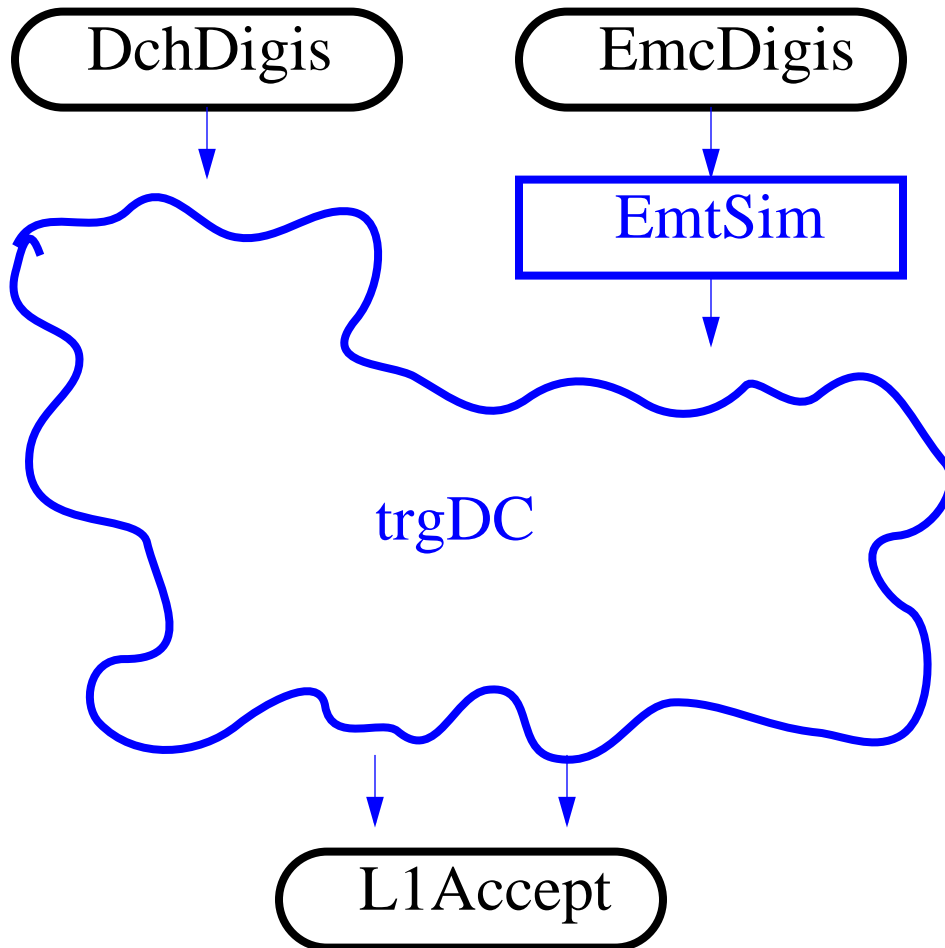
```
L1DTsfHitMaker() {tick loop}
L1DTsfSimModule() {tick loop}
L1DTsfStretcher() {tick loop}
L1DBltReducer() {tick loop}
L1DBltSimModule() {tick loop}
...
```

Subdivided by board and logical operation  
Data held by **class<T> L1SimTimeBuffer**  
and accessed by **class L1SimTickClock**

Data can be dumped or input at any point



## Phase 0 (Now)



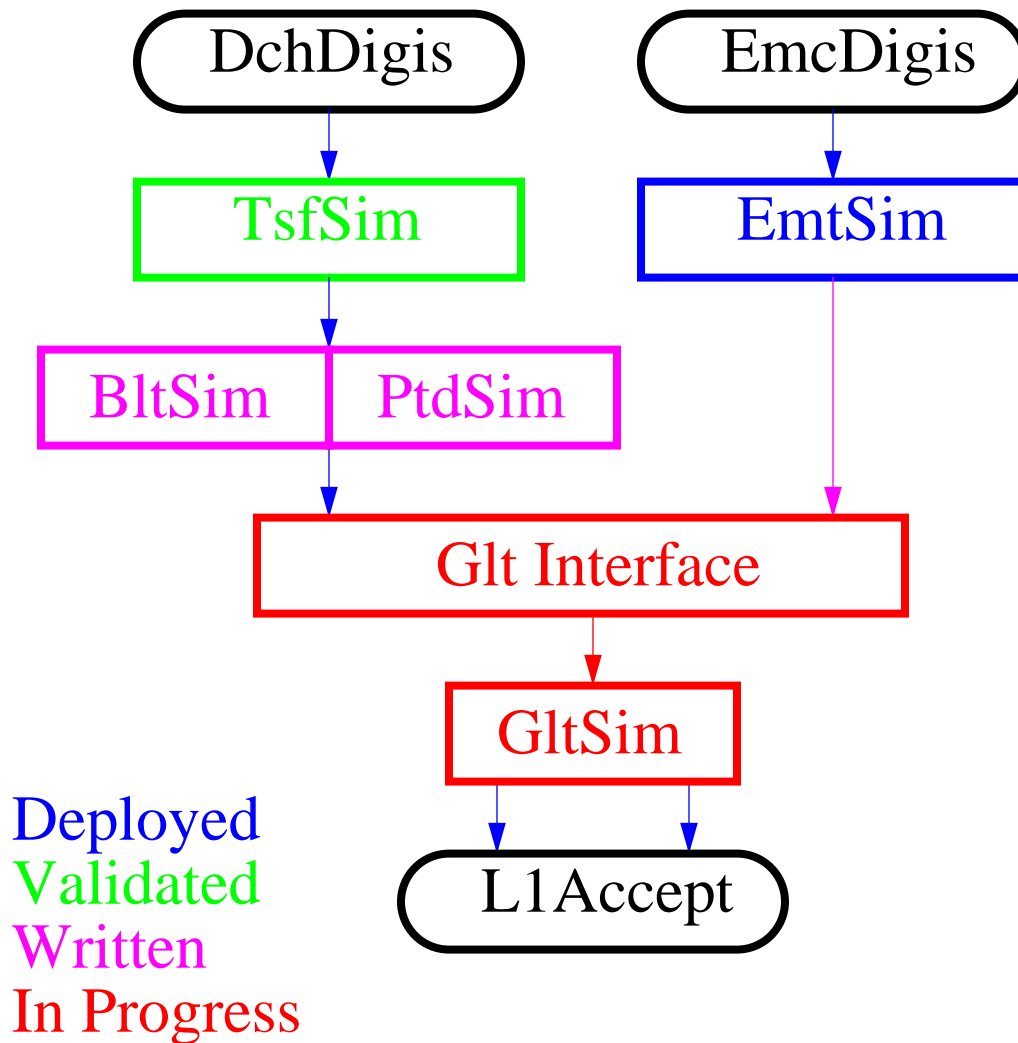
**This IS the current SP6 (14.4.X)**

Base simulation code unchanged,  
but interface elements are new (**Digis, TsfLUT**)

**Remaining changes are inside “black blob”**



# Phase I



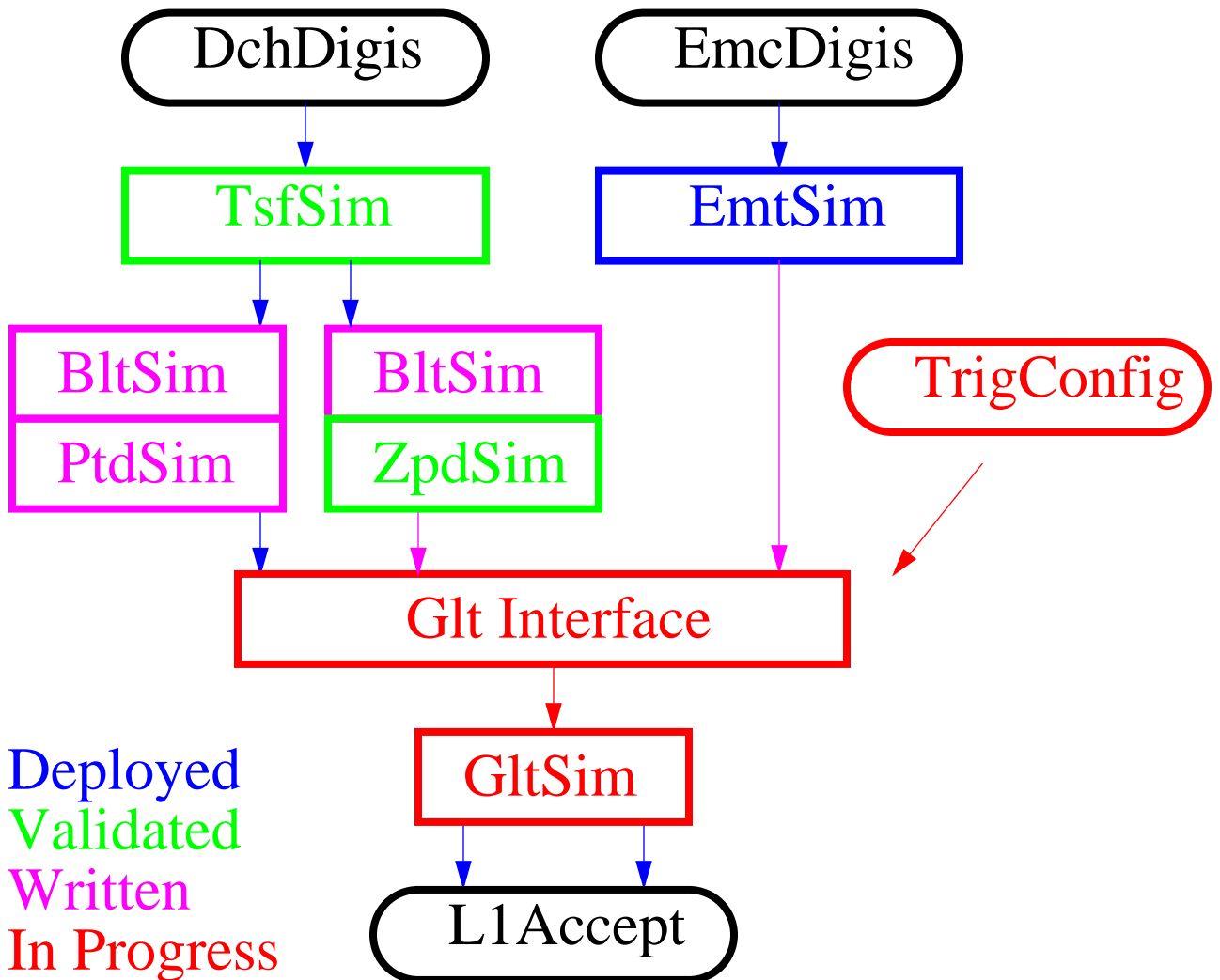
Significant upgrade to existing L1 Simulation

Existing modules (BLT/PTD/GLT)  
turned out to be biggest stumbling block

Unlikely to put Phase I into production...



## Phase II



Full L1Sim upgrade (the final solution)

In principle can be ready shortly after Phase I completed (and validated)



# Simulation Configuration

---



## TSF

- New boards use **6 bit LUT** (current use 5 bit)
- TSF LUT virtual interface now handles this including DB access

## ZPD

- Brand new configuration objects
- Simulation configured from same source as actual hardware
- Still needs to be installed in **configDB**

## BLT/PTD

- BLT mask needs to be put in **configDB**
- PTD will be orphaned and left alone

Essentially all information needed for simulation comes from same source as hardware.



# Global Trigger Configuration

---



## General Question

How to control programmatically in simulation  
the old/new hardware changes?

Need single executable for all data...

## trgConfig

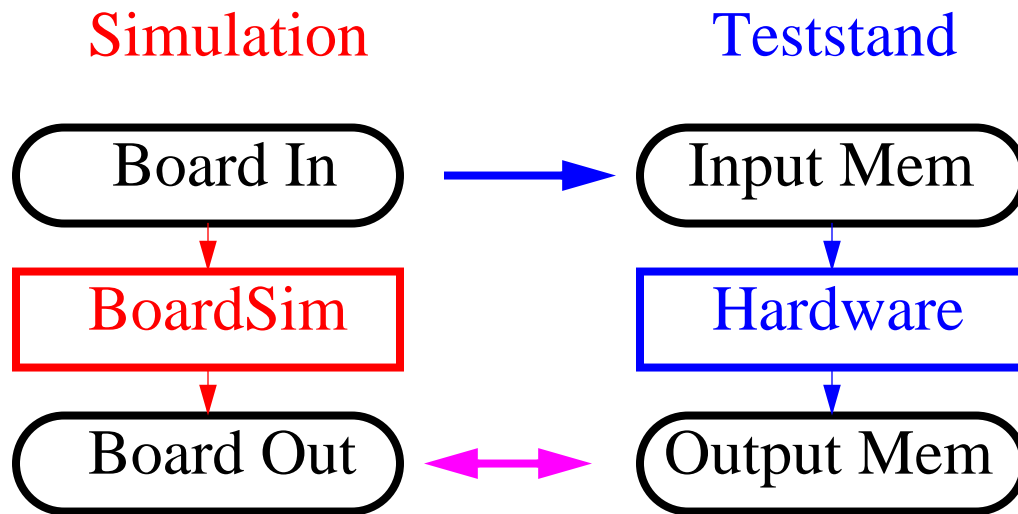
- Define GLT trigger primitive names  
and mapping to specific GLT lines
- Simple changes handled by configDB entries  
for existing cards (i.e. ZPD cuts)
- Firmware/hardware changes will require a  
change to the GLT trigger primitive name

Provides necessary info to switch  
simulation code in an extensible way

trgConfig code coming from Rainer



# Teststand Validation



- Load arbitrary or simulated bit patterns into board memories
- Compare with simulation expectation

## Advantages

Bit-level comparison

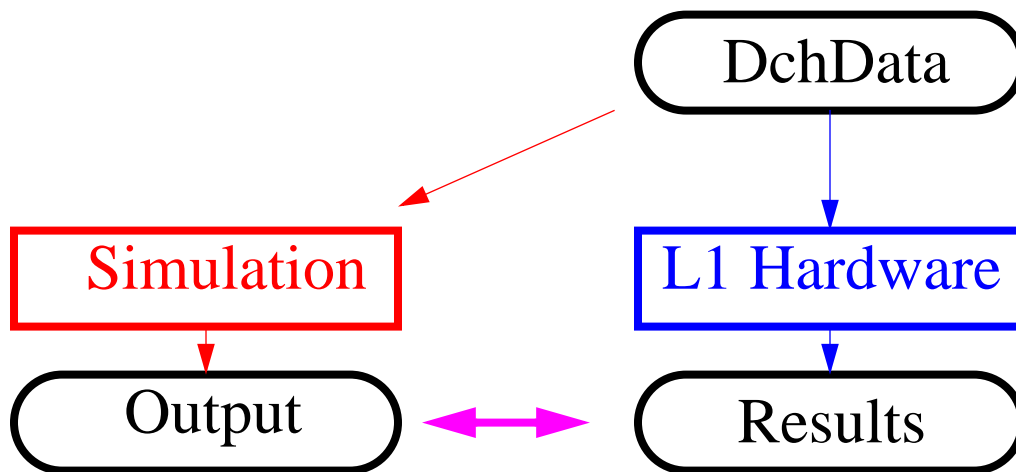
## Disadvantages

Hard to test “system” problems

- Used for new **ZPD**, **TSF**  
Very useful hardware tool, rare errors
- Starting for **BLT**, impossible for **PTD**...



# Data-MC Comparison



- Start with real data (XTC file)
- Compare high-level “physics” output

## Advantages

Straightforward to implement  
Tests “whole system”

Test quantities that really matter?

## Disadvantages

Limited comparisons available (L1Accept)

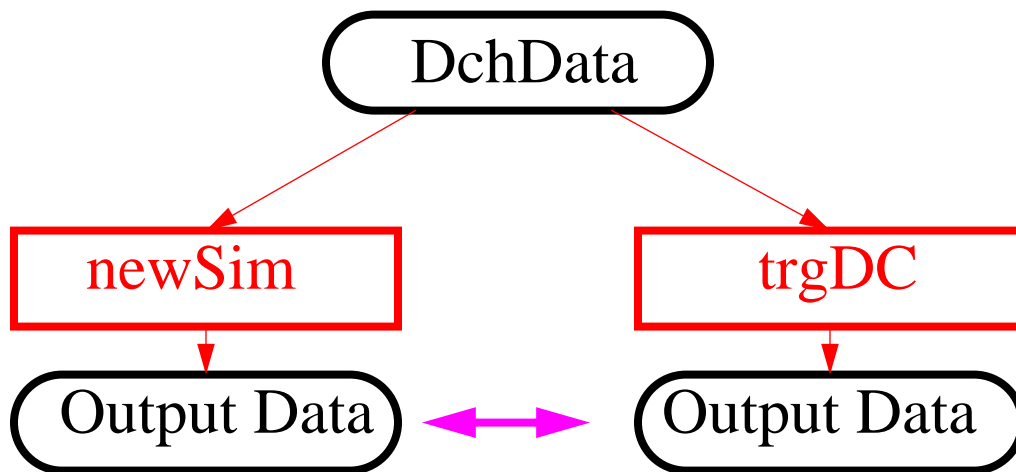
Will not find all problems

Will never find rare/subtle differences

Expand/incorporate into OPRMon package



# trgDC Comparison



- Start with DchDigis (real or simulated)
- Compare parallel simulation output

## Advantages

Tests “whole system”

## Disadvantages

Don't necessarily want agreement!  
Not a direct validation of the hardware

## CM2-Kangerized ‘BogusApp’

In general, want to resurrect the **Bogus/SimApp** model to allow quick simulation of trigger changes in MC without regenerating events...



# Many People

---



## Simulation Upgrade Personnel

- Rainer Bartoldus - trigConfig, stern warnings
  - Nicolas Berger - BLT teststand code
  - Anders Borgland - trgDC keeper
  - Jamie Boyd - TSF sim, general good work
  - Gerald Grenier - teststand and utilities
  - Valerie Halyo - GLT simulation code
  - Olya Igonkina - ZPD simulation code
  - Su Dong - GLT, general whip cracking
  - Eric Torrence - overall feet dragging
- + the L1 hardware upgrade team

Profuse apologies to anybody I forgot...



## A Final Thought

---



Most L1Sim work has been aiming to be ready for new trigger hardware.

New code to be installed in SP7 in time for Run5

Improvements to simulation data/MC agreement and trigger algorithm the longer-term goal.

This work is still to come...